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REV. 4

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC68HC705C8
MC68HC705C4A
MC68HC705C8A
MC68HSC705C8A

Addendum to
MC68HC705C8
HCMOS Microcontroller Unit
Technical Data

This addendum supplements *MC68HC705C8 Technical Data*, Rev. 1 (Motorola document number MC68HC705C8/D) with the following information:

- Corrections to *MC68HC705C8 Technical Data*
- Additional mechanical information for *MC68HC705C8 Technical Data*
- MC68HC705C4A data — APPENDIX A contains data for the MC68HC705C4A, an enhanced version of the MC68HC705C8
- MC68HC705C8A data — APPENDIX B contains data for the MC68HC705C8A, an enhanced version of the MC68HC705C8
- MC68HSC705C8A data — APPENDIX C contains data for the MC68HSC705C8A, a high-speed version of the MC68HC705C8A

CORRECTIONS
MC68HC705C8/D, REV. 1

Corrections to the technical data manual are as follows:

1. Page 2-11, **Figure 2-4. OTPROM/EPROM Programming**:
   a. There should only be one box labeled WAIT 1 ms.
   b. YES label on output of NTRYS = 2 decision box should be NO.

2. Page 3-2, **3.1.3.1 COP RESET REGISTER**: Address of COP reset register should be $001D.

3. Page 3-2, **3.1.3.2 COP CONTROL REGISTER**: The last sentence under the CME bit description should read as follows:

   CME is readable and writable at any time.

4. Page 3-3, **3.1.3.2 COP CONTROL REGISTER**: The second sentence under the CM1 bit description should read as follows:

   CM1 can be read anytime but may be written only once.

5. Page 3-3, **3.1.3.2 COP CONTROL REGISTER**: The second sentence under the CM0 bit description should read as follows:

   CM0 can be read anytime, but may be written only once.

6. Page 3-10, (**3.3.1 STOP Mode**): The first three sentences from the paragraph at the top of the page should read as follows:

   During the STOP mode, the I bit in the CCR is cleared to enable external interrupts.

7. Page 7-9, **Table 7-2. Opcode Map**: Bit Manipulation column heads BTB and BSC should be DIR and DIR.

8. Page 8-1, **8.2 THERMAL CHARACTERISTICS**: Thermal resistance of cerdip package should be 50 °C/W.

9. Page 8-3, **8.4 DC ELECTRICAL CHARACTERISTICS**:
   a. Pins specified under I/O Ports Hi-Z Leakage Current should be PA0–PA7, PB0–PB7, PC0–PC7, PD1–PD4, PD7, $\overline{\text{RESET}}$.
   b. Pins specified under Input Current should be $\overline{\text{IRQ}}$, TCAP, OSC1, PD0, PD5.

10. Page 8-4, **8.5 DC ELECTRICAL CHARACTERISTICS**:

    a. Pins specified under I/O Ports Hi-Z Leakage Current should be
    PA0–PA7, PB0–PB7, PC0–PC7, PD1–PD4, PD7, $\overline{\text{RESET}}$.

    b. Pins specified under Input Current should be
    $\overline{\text{IRQ}}$, TCAP, OSC1, PD0, PD5.

    c. NOTE 3 should be
    Run (Operating) I_{DD} and WAIT I_{DD} measured using external square wave clock source (f_{OSC} = 4.2 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2.

11. Page 8-7, **Figure 8-4. Total Current Drain vs Frequency** (V_{DD} = 3.3 V graph): Internal clock frequencies should read as follows:

    0 250 kHz 500 kHz 750 kHz 1 MHz.

12. Page 8-11, **8.8 SERIAL PERIPHERAL INTERFACE (SPI) TIMING**: Slave enable lag time (Num. 3) should be 720 ns.

13. Page 8-12, **8.8 SERIAL PERIPHERAL INTERFACE (SPI) TIMING**: Slave enable lag time (Num. 3) should be 1500 ns.

ADDITIONAL MECHANICAL DATA
MC68HC705C8 TECHNICAL DATA, REV. 1

The following section supplements SECTION 9 of *MC68HC705C8 Technical Data,* REV. 1 with specifications of the 42-pin shrink dual in-line package (SDIP) and the 44-pin quad flat pack (QFP). The information on pages 9-1 through 9-4 of *MC68HC705C8 Technical Data,* REV. 1 is still valid and **must not be removed**.

SECTION 9
MECHANICAL DATA

9.1 ORDERING INFORMATION

The following table provides additional ordering information for the MC68HC705C8 MCU.

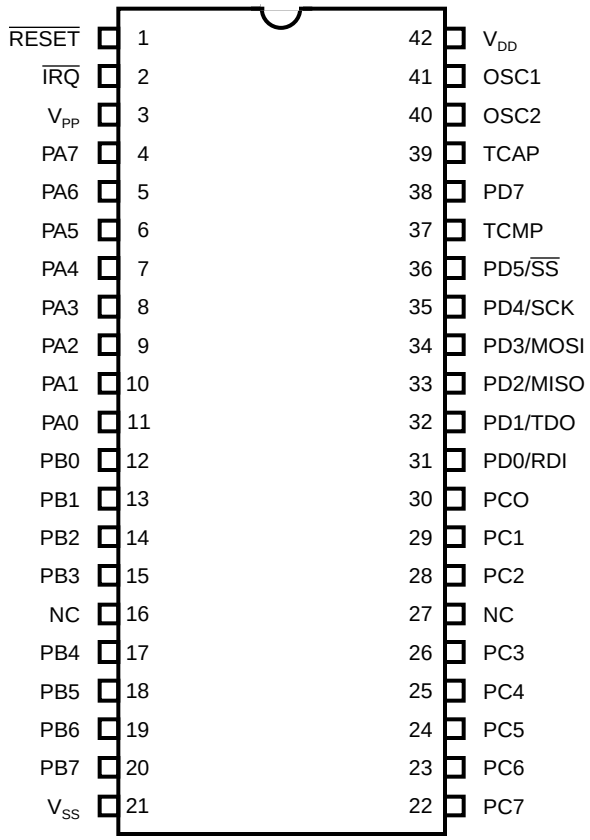
OTPROM MCUs

Package Type	Temperature Range	Order Number
Shrink Dual In-Line Package (SDIP)	0 °C to +70 °C –40 °C to +85 °C	MC68HC705C8B MC68HC705C8CB
Quad Flat Pack (QFP)	0 °C to +70 °C –40 °C to +85 °C	MC68HC705C8FB MC68HC705C8CFB

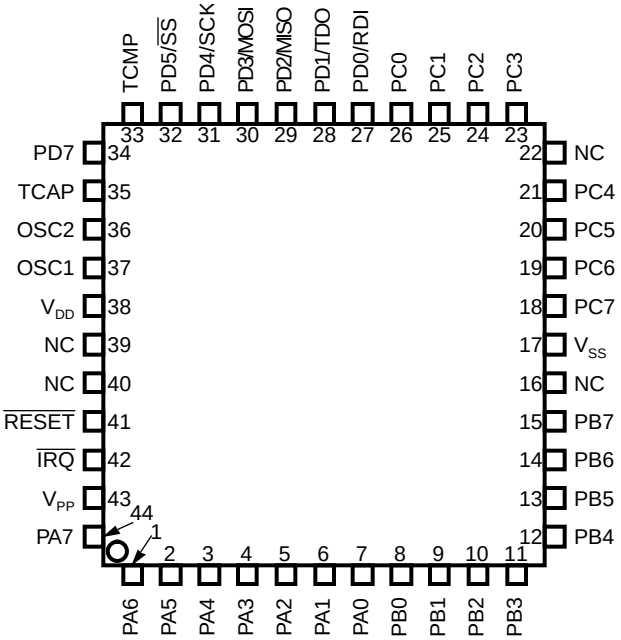
9.2 PIN ASSIGNMENTS

The following figures show the SDIP and QFP pin assignments.

9.2.3 42-Pin SDIP

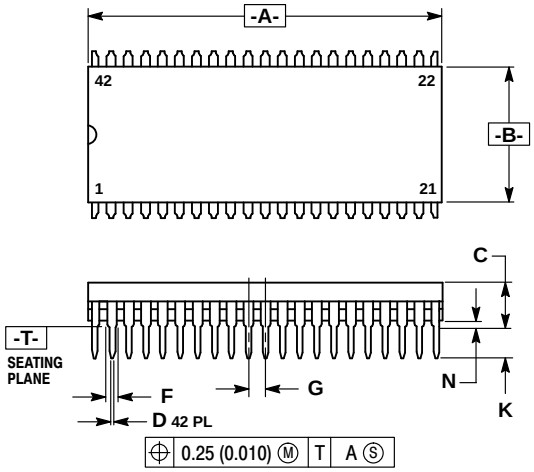


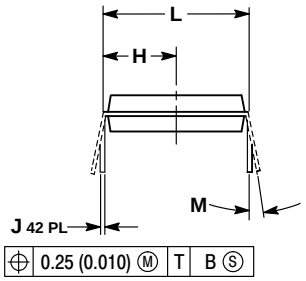
9.2.4 44-Lead QFP



9.3 PACKAGE DIMENSIONS

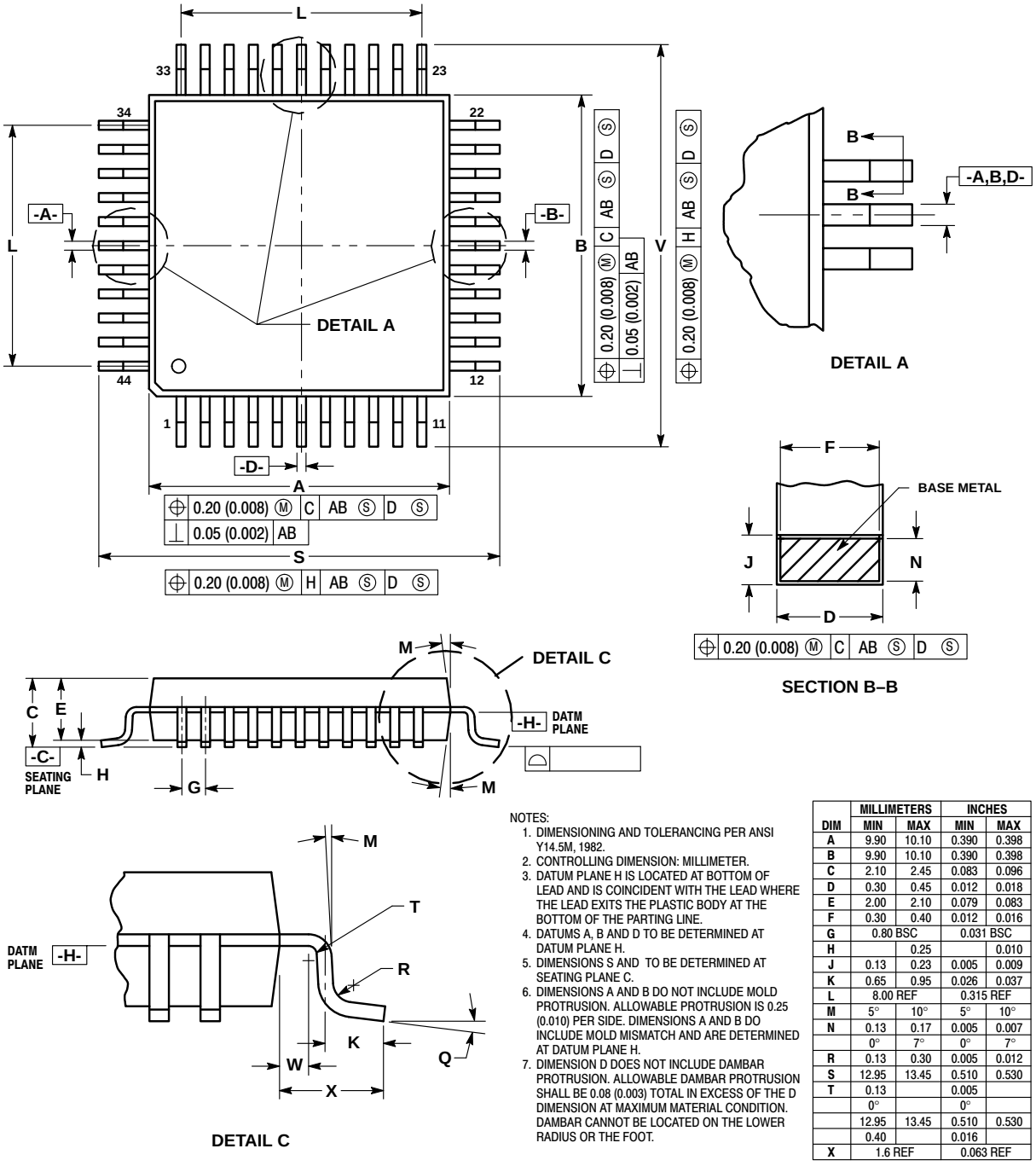
The following figures show the SDIP and QFP dimensions.





NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.032	0.046	0.81	1.17
G	0.070 BSC		1.778 BSC	
H	0.300 BSC		7.62 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS S AND TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.30	0.45	0.012	0.018
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
H		0.25		0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	8.00 REF		0.315 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13		0.005	
	0°		0°	
	12.95	13.45	0.510	0.530
	0.40		0.016	
X	1.6 REF		0.063 REF	

APPENDIX A
MC68HC705C4A

The MC68HC705C4A is an OTPROM/EPROM version of the MC68HC05C4A. Features of the MC68HC705C4A include:

- Mask option registers that control the following:
  - Enabling of port B external interrupt capability
  - Selection of COP watchdog
- High current drive on pin C7

The data in *MC68HC705C8 Technical Data* applies to the MC68HC705C4A with the exceptions given in this appendix.

A.1 MEMORY MAP

Figure A-2 is a memory map of the MC68HC705C4A.

A.2 MASK OPTION REGISTER 1 (MOR1)

MOR1 is an EPROM register that enables the port B pullup devices. Data from MOR1 is latched on the rising edge of the voltage on the $\overline{\text{RESET}}$ pin.

		7	6	5	4	3	2	1	0
MOR1 $1FF0	READ:	PBPU7	PBPU6	PBPU5	PBPU4	PBPU3	PBPU2	PBPU1	PBPU0/ COPC
	WRITE:								
	RESET:	UNAFFECTED BY RESET							
	ERASED:	0	0	0	0	0	0	0	0

Figure A-1. Mask Option Register 1 (MOR1)

PBPU7–PBPU0 — Port B Pullup Bits 7–0

These EPROM bits enable the port B pullup devices.

1 = Port B pullups enabled

0 = Port B pullups disabled

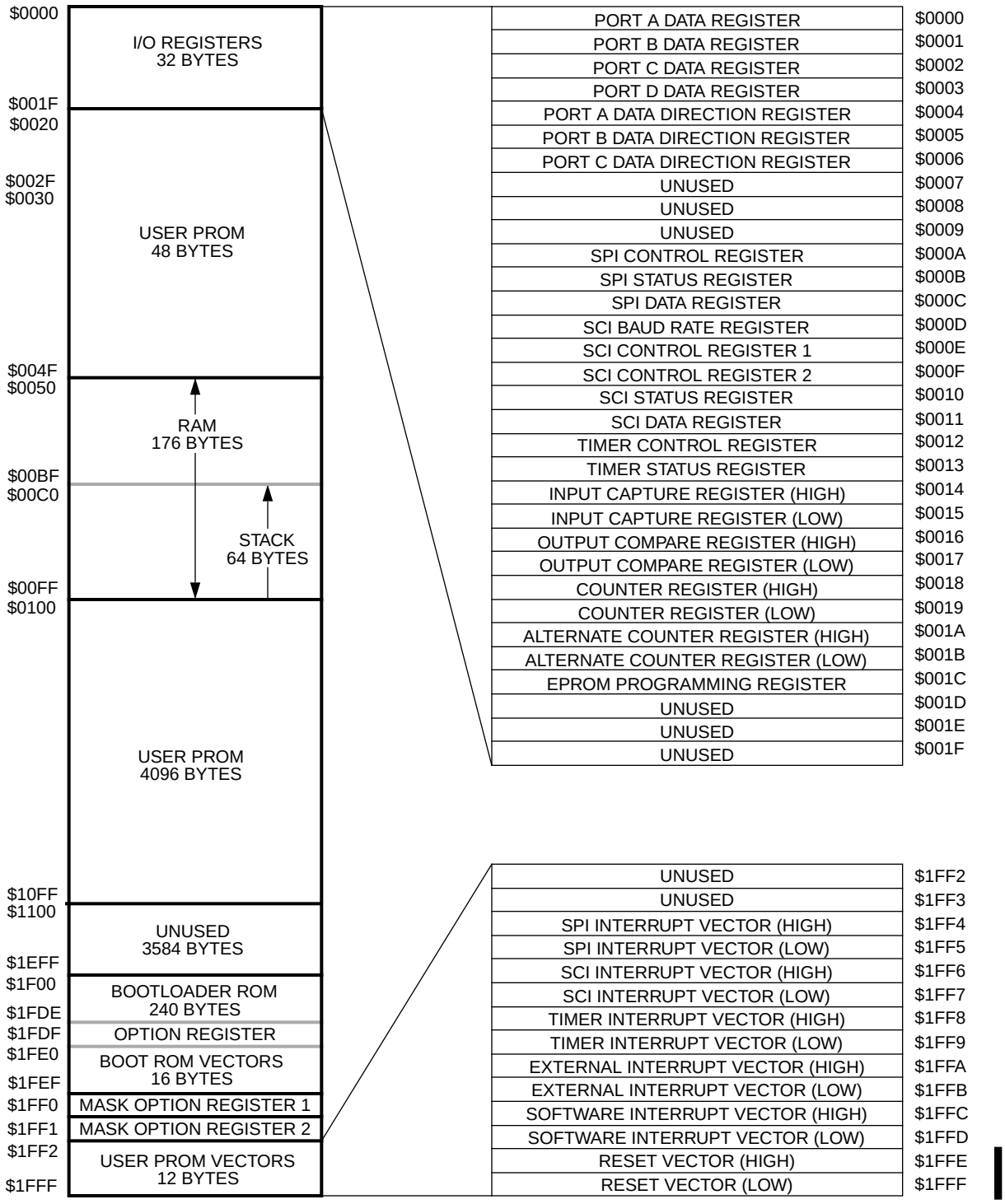


Figure A-2. MC68HC705C4A Memory Map

A.3 MASK OPTION REGISTER 2 (MOR2)

MOR2 is an EPROM register that enables the non-programmable COP watchdog. Data from MOR2 is latched on the rising edge of the voltage on the $\overline{\text{RESET}}$ pin.

		7	6	5	4	3	2	1	0
MOR2 $1FF1	READ:	—	—	—	—	—	—	—	NCOPE
	WRITE:								
	RESET:	UNAFFECTED BY RESET							
	ERASED:	0	0	0	0	0	0	0	0

Figure A-3. Mask Option Register 2 (MOR2)

NCOPE— COP Watchdog Enable

This EPROM bit enables the COP watchdog.

1 = COP watchdog enabled

0 = COP watchdog disabled

A.4 OPTION REGISTER

The option register is used to select the $\overline{\text{IRQ}}$ sensitivity and enable the EPROM security.

	7	6	5	4	3	2	1	0	
$1FDF	0	0	0	0	SEC	—	IRQ	0	**OPTION**
RESET:	0	0	0	0	*	—	1	0	

* The SEC bit is implemented as an EPROM cell.

SEC — Security

This bit is implemented as an EPROM cell and is not affected by reset (U).

1 = Bootloader disabled, MCU operates only in single-chip mode.

0 = Security off, bootloader enabled.

IRQ — Interrupt Request Pin Sensitivity

IRQ is set only by reset, but can be cleared by software. This bit can only be written once.

1 = $\overline{\text{IRQ}}$ pin is both negative edge- and level-sensitive.

0 = $\overline{\text{IRQ}}$ pin is negative edge-sensitive only.

Bits 7, 6, 5, 4, 0 — Not used; these bits always read zero

Bit 2

This bit is not affected by reset (—), and can read either one or zero.

A.5 PORT B EXTERNAL INTERRUPTS

When the following three conditions are true, a port B pin (PBx) acts as an external interrupt pin:

- The corresponding port B pullup bit (PBPUx) in MOR1 is programmed to a logic one.
- The corresponding port B data direction bit (DDRBx) in data direction register B is a logic zero.
- The clear interrupt mask instruction (CLI) has cleared the I bit in the condition code register.

The Port B external interrupt pins can be negative edge-sensitive only or both negative edge- and low level-sensitive, depending on the state of the IRQ bit in the option register (OPTION at location $1FDF). When the IRQ bit is a logic one:

- A falling edge or a low level on a port B external interrupt pin latches an external interrupt request.
- As long as any port B external interrupt pin is low, an external interrupt request is present, and the CPU continues to execute the interrupt service routine.

When the IRQ bit is a logic zero:

- A falling edge on a port B external interrupt pin latches an external interrupt request.
- A subsequent port B external interrupt request can be latched only after the voltage level of the previous port B external interrupt signal returns to a logic one and then falls again to a logic zero. Figure A-4 shows the port B I/O logic.

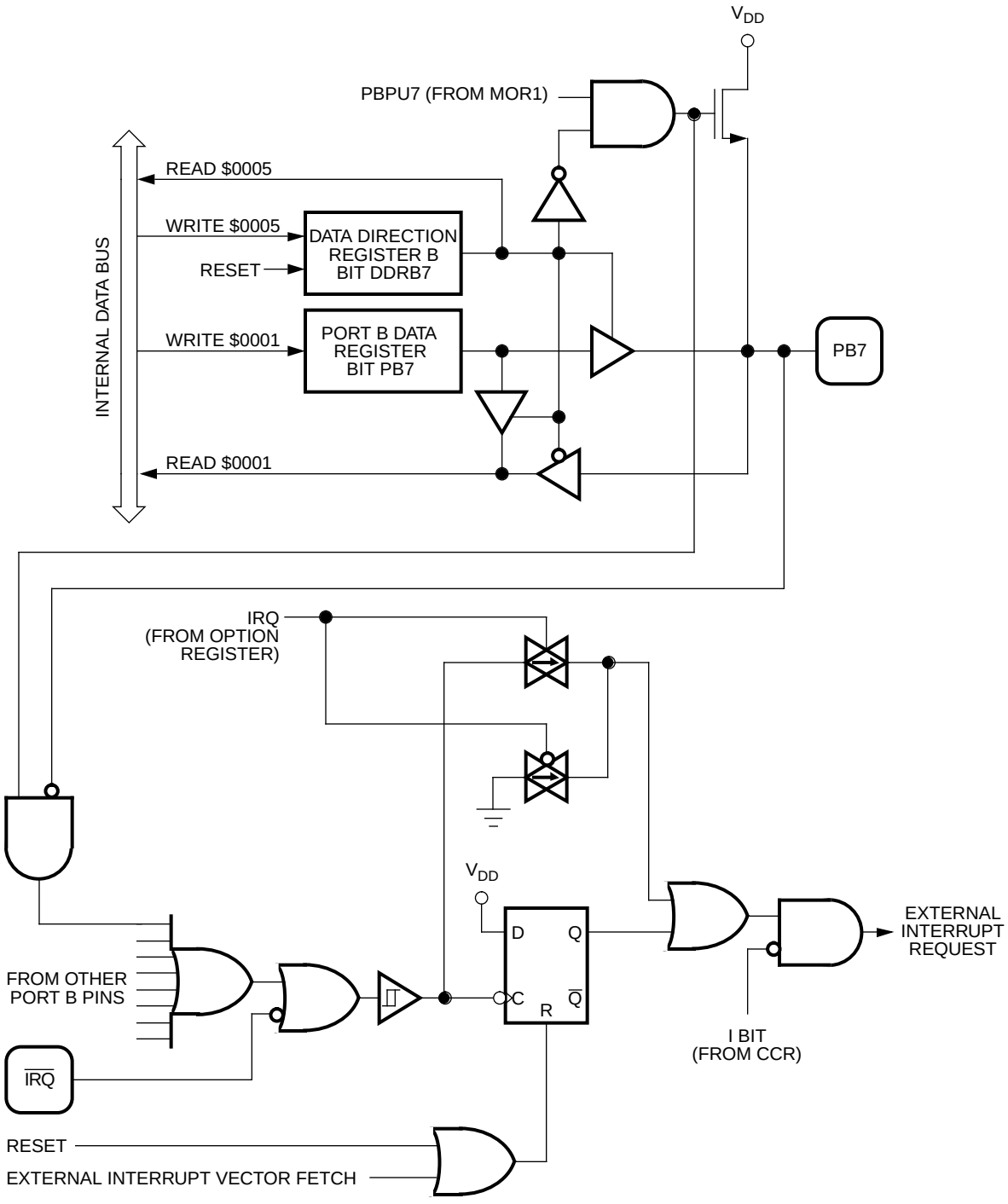


Figure A-4. Port B I/O Logic

A.6 COP WATCHDOG SELECTION

This device includes a watchdog COP feature as a mask register option. The COP is implemented with an 18-bit ripple counter. This provides a timeout period of 64 milliseconds at a bus rate of 2 MHz. If the COP should time out, a system reset will occur and the device will be re-initialized in the same fashion as a POR or external reset.

A timeout of the 18-stage ripple counter generates a reset. The timeout period when f_{osc} = 4 MHz is 64 ms. Two memory locations control operation of the COP:

- The COP enable bit (NCOPE) in mask option register 2 (MOR2) — Programming the NCOPE bit in MOR2 to a logic one enables the COP watchdog.
- The COP clear bit (COPC) at address $1FF0 — To clear the COP and start a new timeout period, write a logic zero to bit 0 of address $1FF0. Reading address $1FF0 returns the mask option register 1 (MOR1) data at that location. (See **A.2 MASK OPTION REGISTER 1 (MOR1)**.)

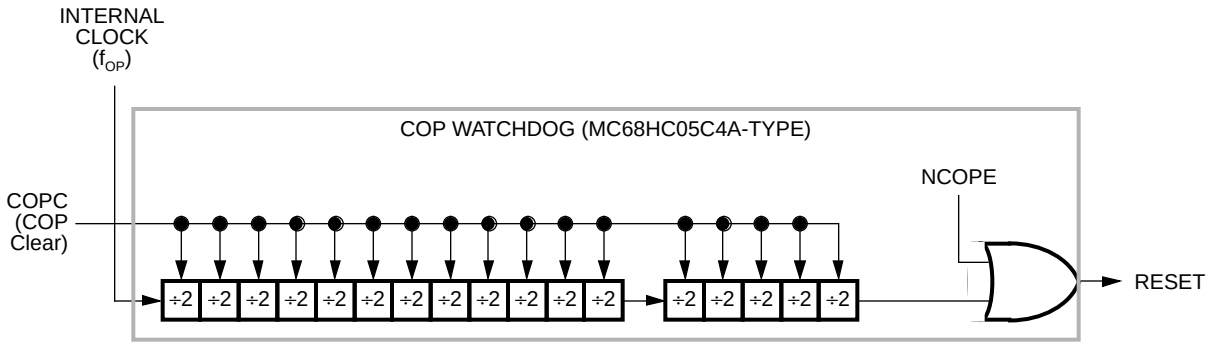


Figure A-5. MC68HC705C4A COP Watchdog

A.6.1 COP Watchdog in WAIT Mode

The COP will continue to operate normally during WAIT mode. To prevent a COP reset, the software should pull the device out of WAIT mode periodically and reset the COP by writing to bit 0 of address $1FF0.

A.6.2 COP Watchdog in STOP Mode

The STOP instruction has the following effects on the COP watchdog:

- Turns off the oscillator and turns off the COP watchdog counter
- Clears the COP watchdog counter

If the $\overline{\text{RESET}}$ pin brings the MCU out of STOP mode, the COP watchdog begins counting immediately. The reset function clears the COP counter again after the 4064-t_{CYC} clock stabilization delay.

If the $\overline{\text{IRQ}}$ pin brings the MCU out of STOP mode, the COP watchdog begins counting immediately. The IRQ function does not clear the COP counter again after the 4064-t_{CYC} clock stabilization delay. See Figure A-6.

NOTE

If the clock monitor is enabled (CME = 1), the STOP instruction causes it to time out and reset the MCU.

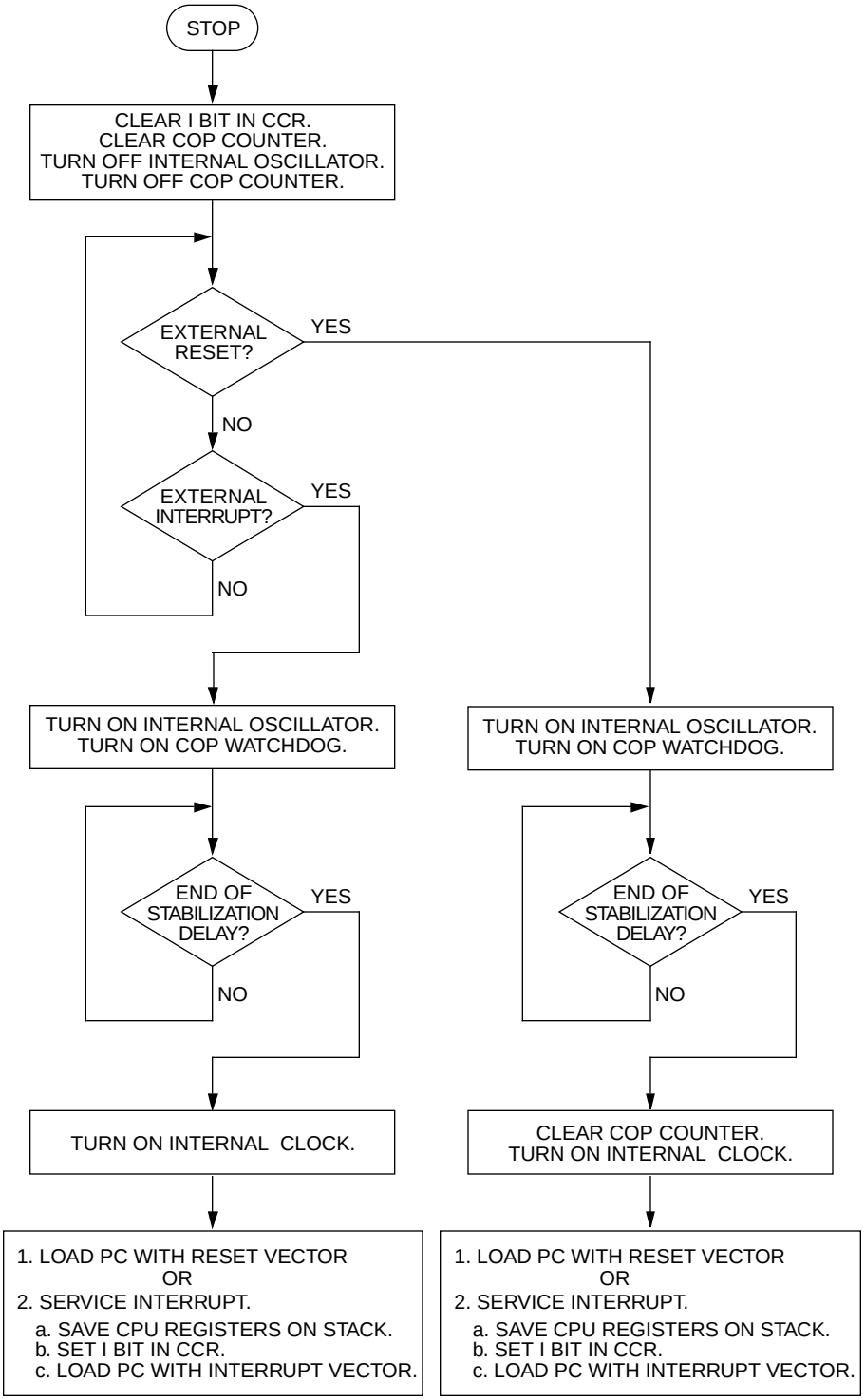


Figure A-6. COP Watchdog in STOP Mode (NCOPE = 1)

A.7 DC ELECTRICAL CHARACTERISTICS

Table A-1. DC Electrical Characteristics (V_{DD} = 5.0 V ± 10%)

Characteristic	Symbol	Min	Typ(1)	Max	Unit
Output High Voltage					
I_{LOAD} = –0.8 mA					
PA7–PA0, PB7–PB0, PC6–PC0, TCMP	V_{OH}	V_{DD} – 0.8	—	—	V
I_{LOAD} = –1.6 mA					
PD4–PD1		V_{DD} – 0.8	—	—	V
I_{LOAD} –5.0 mA					
PC7		V_{DD} – 0.8	—	—	V
Output Low Voltage					
I_{LOAD} = 1.6 mA					
PA7–PA0, PB7–PB0, PC6–PC0, PD4–PD1	V_{OL}	—	—	0.4	V
I_{LOAD} = 20 mA					
PC7		—	—	0.4	V
Supply Current(2)					
Run(3)		—	2.78	7.0	mA
WAIT(4)		—	1.86	3.0	mA
STOP(5)	I_{DD}				
25 °C		—	5.0	50	µA
–40 °C to +85 °C		—	5.0	50	µA
EPROM Programming Voltage	V_{PP}	16.0	16.25	16.5	V

1. Typical values reflect average measurements at midpoint of voltage range at 25 °C.
2. I_{DD} measured with port B pullup devices disabled.
3. Run (operating) I_{DD} measured using external square wave clock source (f_{OSC} = 4.2 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2.
4. WAIT I_{DD} measured using external square wave clock source (f_{OSC} = 4.2 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2. V_{IL} = 0.2 V, V_{IH} = V_{DD} – 0.2 V. All ports configured as inputs. SPI and SCI disabled. If SPI and SCI enabled, add 10% current draw. OSC2 capacitance linearly affects WAIT I_{DD}.
5. STOP I_{DD} measured with OSC1 = V_{DD}. All ports configured as inputs. V_{IL} = 0.2 V, V_{IH} = V_{DD} – 0.2 V.

Table A-2. DC Electrical Characteristics (V_{DD} = 3.3 V ± 10%)

Characteristic	Symbol	Min	Typ(1)	Max	Unit
Output High Voltage I_{LOAD} = –0.2 mA PA7–PA0, PB7–PB0, PC6–PC0, TCMP I_{LOAD} = –0.4 mA PD4–PD1 I_{LOAD} = –1.5 mA PC7	V_{OH}	 V_{DD} – 0.3 V_{DD} – 0.3 V_{DD} – 0.3	 — — —	 — — —	 V V V
Output Low Voltage I_{LOAD} = 0.4 mA PA7–PA0, PB7–PB0, PC6–PC0, PD4–PD1 I_{LOAD} = 6.0 mA PC7	V_{OL}	 — —	 — —	 0.3 0.3	 V V
Supply Current Run(2) WAIT(3) STOP(4)	I_{DD}	 — — —	 1.51 0.972 2.0	 3.0 1.0 20	 mA mA µA

1. Typical values reflect average measurements at midpoint of voltage range at 25 °C.
2. Run (operating) I_{DD} measured using external square wave clock source (f_{OSC} = 2.0 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2.
3. WAIT I_{DD} measured using external square wave clock source (f_{OSC} = 2.0 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2. V_{IL} = 0.2 V, V_{IH} = V_{DD} – 0.2 V. All ports configured as inputs. SPI and SCI disabled. If SPI and SCI enabled, add 10% current draw. OSC2 capacitance linearly affects WAIT I_{DD}.
4. STOP I_{DD} measured with OSC1 = V_{DD}. All ports configured as inputs. V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V.

A.8 ORDERING INFORMATION

Table B-6 provides ordering information for the MC68HC705C4A.

Table A-3. MC68HC705C4A Order Numbers

Package Type	Temperature Range	Order Number
40-Pin Plastic Dual In-Line Package (DIP)	0 °C to +70 °C –40 °C to +85 °C	MC68HC705C4AP(1) MC68HC705C4AC(2)P
44-Lead Plastic-Leaded Chip Carrier (PLCC)	0 °C to +70 °C –40 °C to +85 °C	MC68HC705C4AFN(3) MC68HC705C4ACFN
44-Lead Quad Flat Pack (QFP)	0 °C to +70 °C –40 °C to +85 °C	MC68HC705C4AFB(4) MC68HC705C4ACFB
42-Pin Shrink Dual In-Line Package (SDIP)	0 °C to +70 °C –40 °C to +85 °C	MC68HC705C4AB(5) MC68HC705C4ACB

1. P = Plastic dual in-line package (DIP).
2. C = Extended temperature range (–40 °C to +85 °C).
3. FN = Plastic-leaded chip carrier (PLCC).
4. FB = 10 mm × 10 mm quad flat pack (QFP).
5. B = Shrink dual in-line plastic (SDIP).

A.9 PIN ASSIGNMENTS

A.9.1 DIP (MC68HC705C4AP)

MC68HC705C4AP pin assignments are identical to those of the MC68HC705C8P.

A.9.2 PLCC (MC68HC705C4AFN)

MC68HC705C4AFN pin assignments are identical to those of the MC68HC705C8FN.

A.9.3 QFP (MC68HC705C4AFB)

MC68HC705C4AFB pin assignments, shown in Figure A-7, are identical to those of the MC68HC705C8FB.

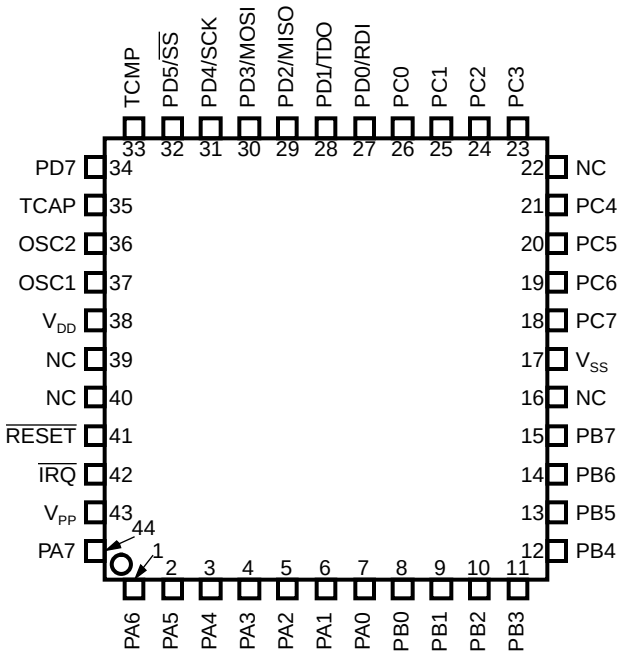


Figure A-7. MC68HC705C4AFN Pin Assignments

A.9.4 SDIP (MC68HC705C4AB)

MC68HC705C4AB pin assignments, shown in Figure A-8, are identical to those of the MC68HC705C8B.

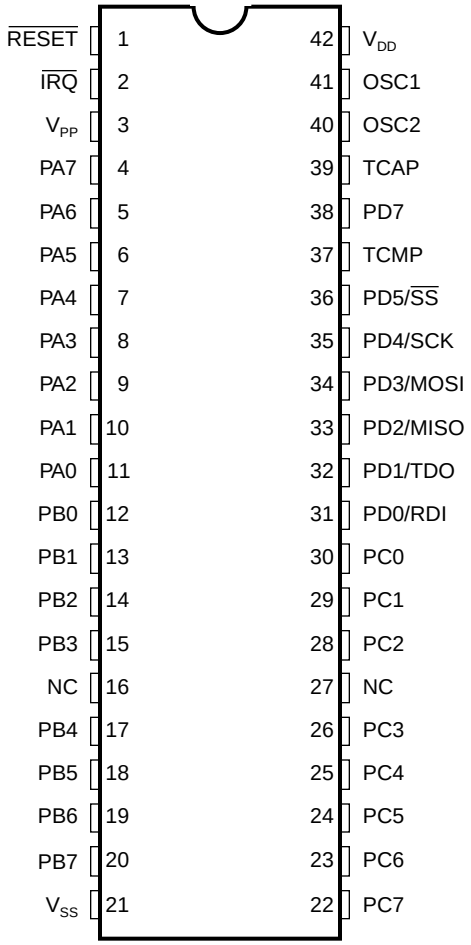


Figure A-8. MC68HC705C4AB Pin Assignments

A.10 PACKAGE DIMENSIONS

A.10.1 DIP (MC68HC705C4AP)

MC68HC705C4AP dimensions are identical to those of the MC68HC705C8P.

A.10.2 PLCC (MC68HC705C4AFN)

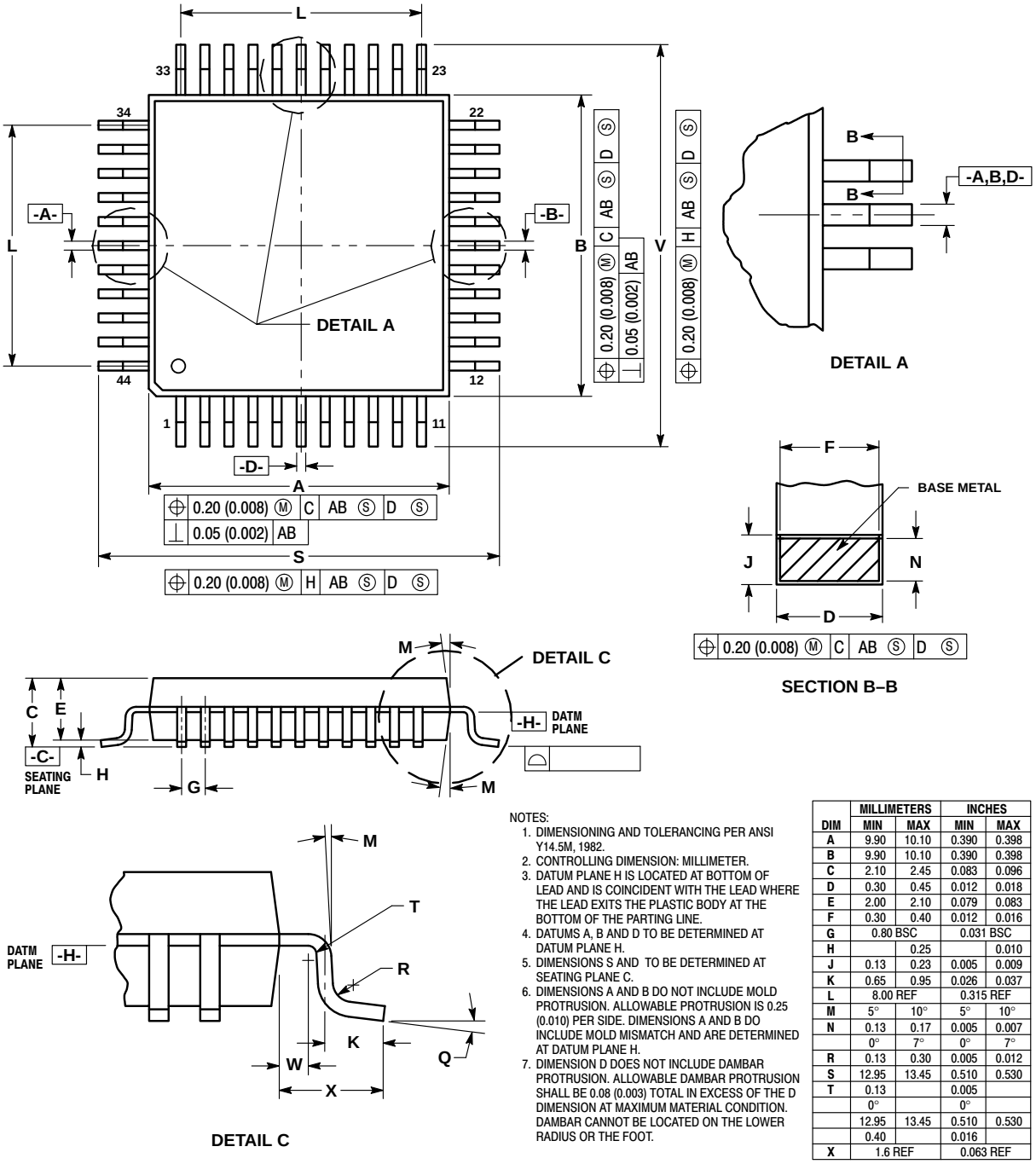
MC68HC705C4AFN dimensions are identical to those of the MC68HC705C8FN.

A.10.3 QFP (MC68HC705C4AFB)

MC68HC705C4AFB dimensions, shown in Figure A-9, are identical to those of the MC68HC705C8FB.

A.10.4 SDIP (MC68HC705C4AB)

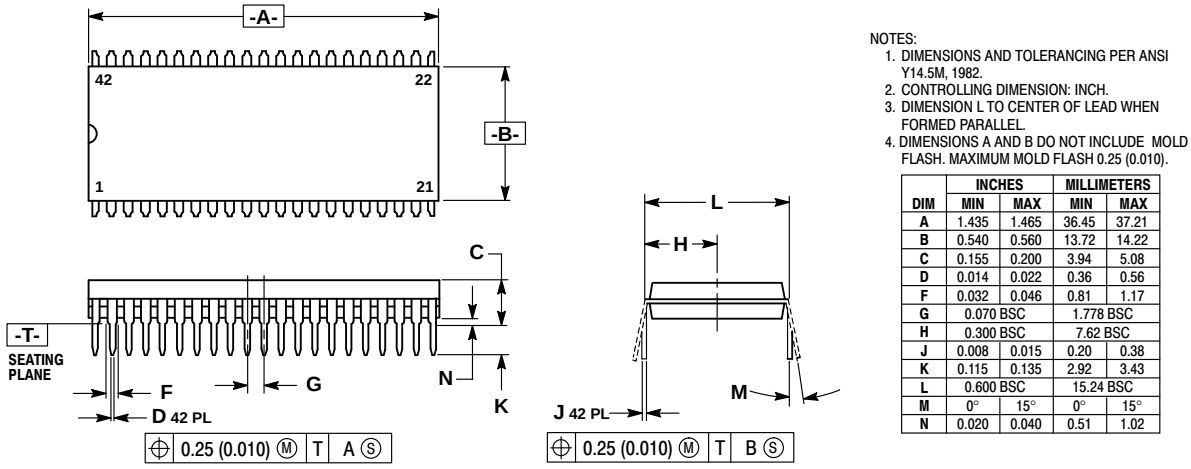
MC68HC705C4AB dimensions, shown in Figure A-10, are identical to those of the MC68HC705C8B.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS S AND TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.30	0.45	0.012	0.018
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
H		0.25		0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	8.00 REF		0.315 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13		0.005	
	0°		0°	
	12.95	13.45	0.510	0.530
	0.40		0.016	
X	1.6 REF		0.063 REF	

Figure A-9. MC68HC705C4AFB Package Dimensions



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.032	0.046	0.81	1.17
G	0.070 BSC		1.778 BSC	
H	0.300 BSC		7.62 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

Figure A-10. MC68HC705C4AB Package Dimensions

APPENDIX B
MC68HC705C8A

The MC68HC705C8A is an enhanced version of the MC68HC705C8. Features of the MC68HC705C8A include:

- Mask option registers that control the following:
  - Enabling of port B external interrupt capability
  - Selection of programmable and/or non-programmable COP watchdogs
- High current drive on pin C7

The data in *MC68HC705C8 Technical Data,* REV. 1 applies to the MC68HC705C8A with the exceptions given in this appendix.

B.1 MEMORY MAP

Figure B-2 is a memory map of the MC68HC705C8A.

B.2 MASK OPTION REGISTER 1 (MOR1)

MOR1 is an EPROM register that enables the port B pullup devices. Data from MOR1 is latched on the rising edge of the voltage on the $\overline{\text{RESET}}$ pin.

		7	6	5	4	3	2	1	0
MOR1 $1FF0	READ:	PBPU7	PBPU6	PBPU5	PBPU4	PBPU3	PBPU2	PBPU1	PBPU0/ COPC
	WRITE:								
	RESET:	UNAFFECTED BY RESET							
	ERASED:	0	0	0	0	0	0	0	0

Figure B-1. Mask Option Register 1 (MOR1)

PBPU7–PBPU0 — Port B Pullup Enable Bits 7–0
These EPROM bits enable the port B pullup devices.
1 = Port B pullups enabled
0 = Port B pullups disabled

NOTE

PBPU0/COPC programmed to a one enables the port B pullup bit. This bit is also used to clear the non-programmable COP (C4A type). Writing to this bit to clear the COP will not affect the state of the port B pullup (bit 0). (See **B.5.2 Non-Programmable COP Watchdog**.)

NOTE

When using the MC68HC705C8A in an MC68HC705C8 or MC68HSC705C8 application, program locations $1FF0 and $1FF1 to $00.

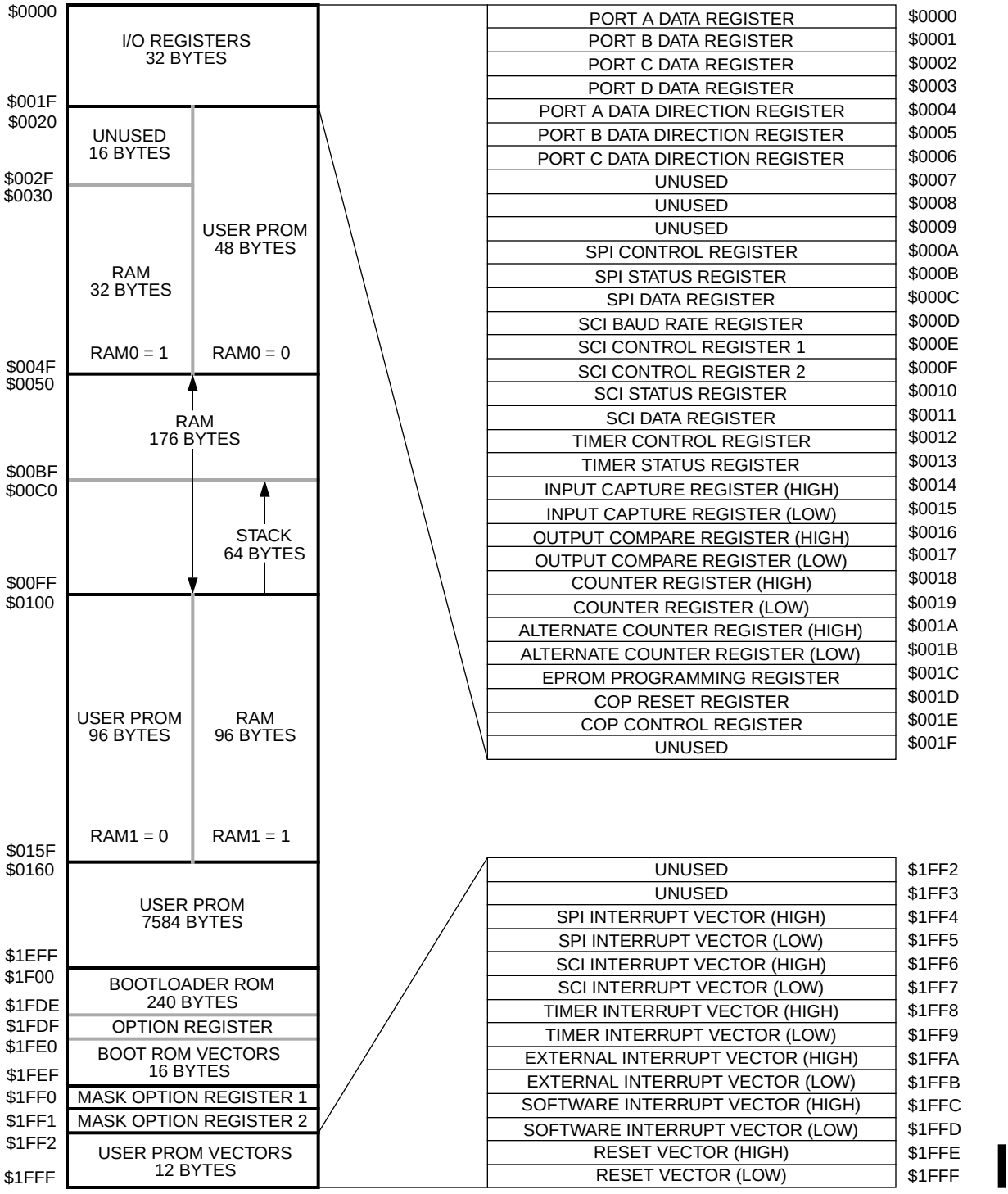


Figure B-2. MC68HC705C8A Memory Map

B.3 MASK OPTION REGISTER 2 (MOR2)

MOR2 is an EPROM register that enables the non-programmable COP watchdog. Data from MOR2 is latched on the rising edge of the voltage on the $\overline{\text{RESET}}$ pin.

		7	6	5	4	3	2	1	0
MOR2 $1FF1	READ:	—	—	—	—	—	—	—	NCOPE
	WRITE:								
	RESET:	UNAFFECTED BY RESET							
	ERASED:	0	0	0	0	0	0	0	0

Figure B-3. Mask Option Register 2 (MOR2)

NCOPE— Non-Programmable COP Watchdog Enable

This EPROM bit enables the non-programmable COP watchdog.

1 = Non-programmable COP watchdog enabled

0 = Non-programmable COP watchdog disabled

B.4 PORT B EXTERNAL INTERRUPTS

When the following three conditions are true, a port B pin (PBx) acts as an external interrupt pin:

- The corresponding port B pullup bit (PBPUx) in MOR1 is programmed to a logic one.
- The corresponding port B data direction bit (DDRBx) in data direction register B is a logic zero.
- The clear interrupt mask instruction (CLI) has cleared the I bit in the condition code register.

The Port B external interrupt pins can be negative edge-sensitive only or both negative edge- and low level-sensitive, depending on the state of the IRQ bit in the option register (OPTION at location $1FDF). When the IRQ bit is a logic one:

- A falling edge or a low level on a port B external interrupt pin latches an external interrupt request.
- As long as any port B external interrupt pin is low, an external interrupt request is present, and the CPU continues to execute the interrupt service routine.

When the IRQ bit is a logic zero:

- A falling edge on a port B external interrupt pin latches an external interrupt request.
- A subsequent port B external interrupt request can be latched only after the voltage level of the previous port B external interrupt signal returns to a logic one and then falls again to a logic zero. Figure B-4 shows the port B I/O logic.

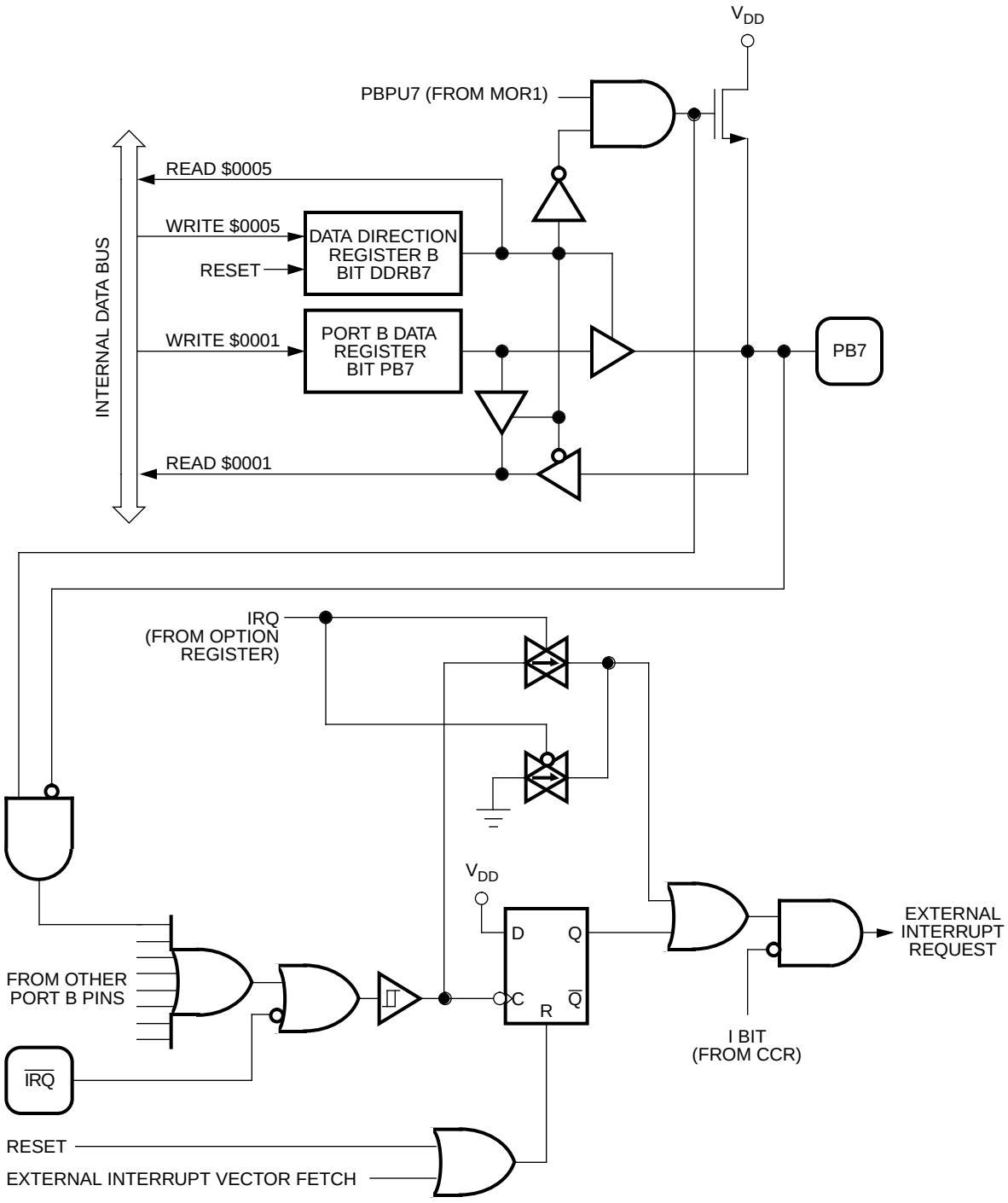


Figure B-4. Port B I/O Logic

B.5 COP WATCHDOG SELECTION

For COP watchdog application compatibility with devices such as the MC68HC705C8 and MC68HC05C4A, the MC68HC705C8A has two different COP watchdogs. One COP watchdog has four programmable timeout periods, and the other has a fixed, non-programmable timeout period. Figure B-5 is a block diagram of the two COP watchdogs.

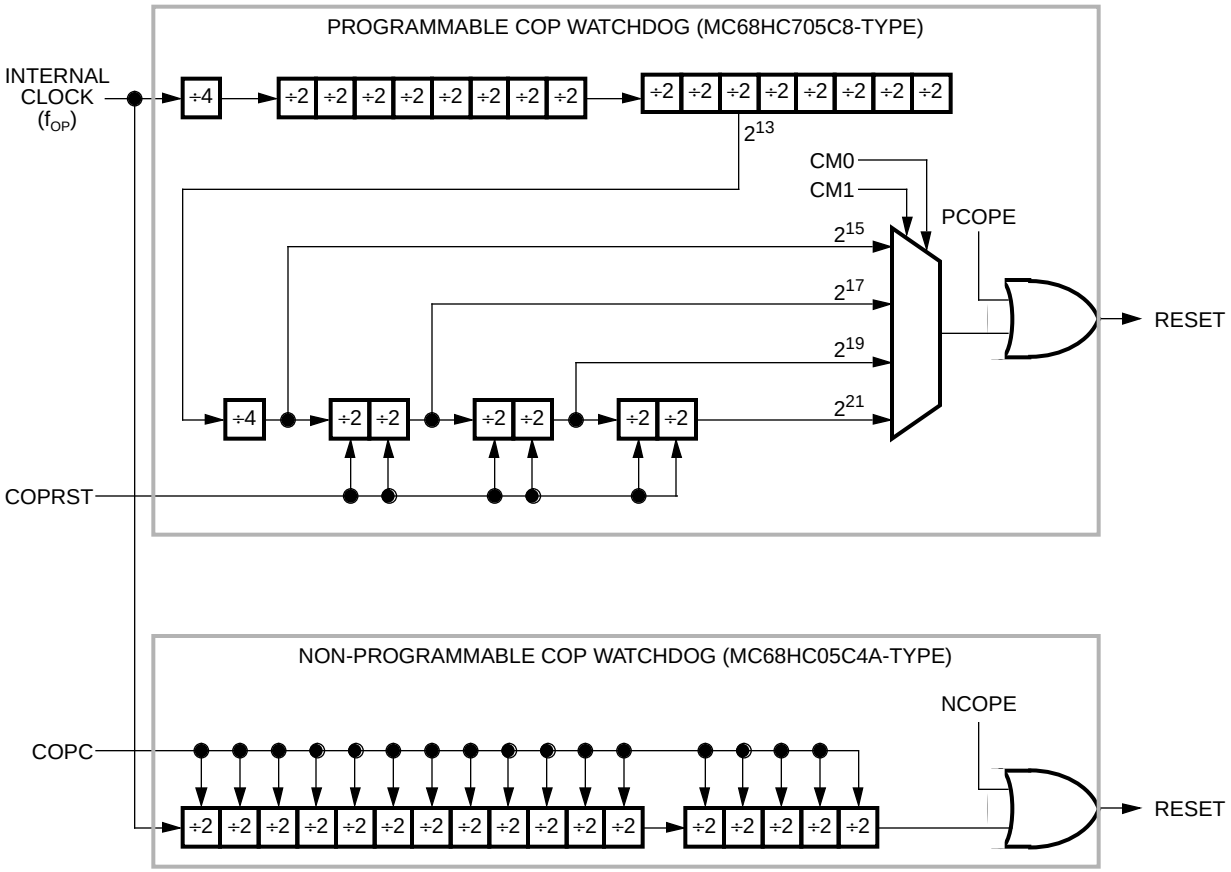


Figure B-5. MC68HC705C8A COP Watchdogs

B.5.1 Programmable COP Watchdog

A timeout of the 18-stage ripple counter in the programmable COP watchdog generates a reset. Two registers control and monitor operation of the programmable COP watchdog:

- COP reset register
- COP control register

B.5.1.1 COP Reset Register (COPRST)

To clear the programmable COP watchdog and begin a new timeout period, write the following values to the COP reset register:

1. $55
2. $AA

The $55 write must precede the $AA write. Instructions may be executed between the write operations provided that the COP watchdog does not time out before the second write.

		7	6	5	4	3	2	1	0
COPRST $001D	READ:								
	WRITE:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RESET:	X	X	X	X	X	X	X	X

X = INDETERMINATE

Figure B-6. COP Reset Register (COPRST)

B.5.1.2 COP Control Register (COPCR)

The COP control register does the following:

- Flags programmable COP watchdog resets
- Enables the clock monitor
- Enables the programmable COP watchdog
- Controls the timeout period of the programmable COP watchdog

		7	6	5	4	3	2	1	0
COPCR $001E	READ:	0	0	0	COPF	CME	PCOPE	CM1	CM0
	WRITE:								
	RESET:	0	0	0	U	0	0	0	0

U = UNAFFECTED

Figure B-7. COP Control Register (COPCR)

Bits 7–5 — Unused

Bits 7–5 always read as logic zeros. Reset clears bits 7–5.

COPF — COP Flag

This read-only bit is set when a timeout of the programmable COP watchdog occurs or when the clock monitor detects a slow or absent internal clock. Clear the COPF bit by reading the COP control register. Reset has no effect on the COPF bit.

1 = COP timeout or internal clock failure
0 = No COP timeout and no internal clock failure

CME — Clock Monitor Enable

This read/write bit enables the clock monitor. The clock monitor sets the COPF bit and generates a reset if it detects an absent internal clock for a period of from 5 μs to 100 μs. The CME bit is readable at any time but can be written only once after reset. Reset clears the CME bit.

1 = Clock monitor enabled
0 = Clock monitor disabled

NOTE

Do not enable the clock monitor in applications with an internal clock frequency of 200 kHz or less.

If the clock monitor detects a slow clock, it drives the bidirectional $\overline{\text{RESET}}$ pin low for four clock cycles. If the clock monitor detects an absent clock, it drives the $\overline{\text{RESET}}$ pin low until the clock recovers.

PCOPE — Programmable COP Enable

This read/write bit enables the programmable COP watchdog. PCOPE is readable at any time but can be written only once after reset. Reset clears the PCOPE bit.

1 = Programmable COP watchdog enabled
0 = Programmable COP watchdog disabled

NOTE

Programming the non-programmable COP enable bit (NCOPE) in mask option register 2 (MOR2) to logic one enables the non-programmable COP watchdog. Setting the PCOPE bit while the NCOPE bit is programmed to logic one enables both COP watchdogs to operate at the same time.

CM1 and CM0 — COP Mode Bits

These read/write bits select the timeout period of the programmable COP watchdog as shown in Table B-1. CM1 and CM0 can be cleared only by reset. Reset clears the CM1 and CM0 bits.

Table B-1. Programmable COP Timeout Period Selection

CM1:CM0	COP Timeout Rate	Programmable COP Timeout Period			
		f_{OSC} = 4.0 MHz f_{OP} = 2.0 MHz	f_{OSC} = 3.5795 MHz f_{OP} = 1.7897 MHz	f_{OSC} = 2.0 MHz f_{OP} = 1.0 MHz	f_{OSC} = 1.0 MHz f_{OP} = 0.5 MHz
00	$f_{OP} \div 2^{15}$	16.38 ms	18.31 ms	32.77 ms	65.54 ms
01	$f_{OP} \div 2^{17}$	65.54 ms	73.24 ms	131.07 ms	262.14 ms
10	$f_{OP} \div 2^{19}$	262.14 ms	292.95 ms	524.29 ms	1.048 s
11	$f_{OP} \div 2^{21}$	1.048 s	1.172 s	2.097 s	4.194 s

B.5.1.3 Programmable COP Watchdog in WAIT Mode

The programmable COP watchdog is active during WAIT mode. Software must periodically bring the MCU out of WAIT mode to clear the programmable COP watchdog.

B.5.1.4 Programmable COP Watchdog in STOP Mode

The STOP instruction turns off the internal oscillator and suspends the COP watchdog counter. If the $\overline{\text{RESET}}$ pin brings the MCU out of STOP mode, the reset function clears and disables the COP watchdog.

If the $\overline{\text{IRQ}}$ pin brings the MCU out of STOP mode, the COP counter resumes counting from its suspended value after the 4064-t_{CYC} clock stabilization delay. See Figure B-8.

NOTE

If the clock monitor is enabled (CME = 1), the STOP instruction causes it to time out and reset the MCU.

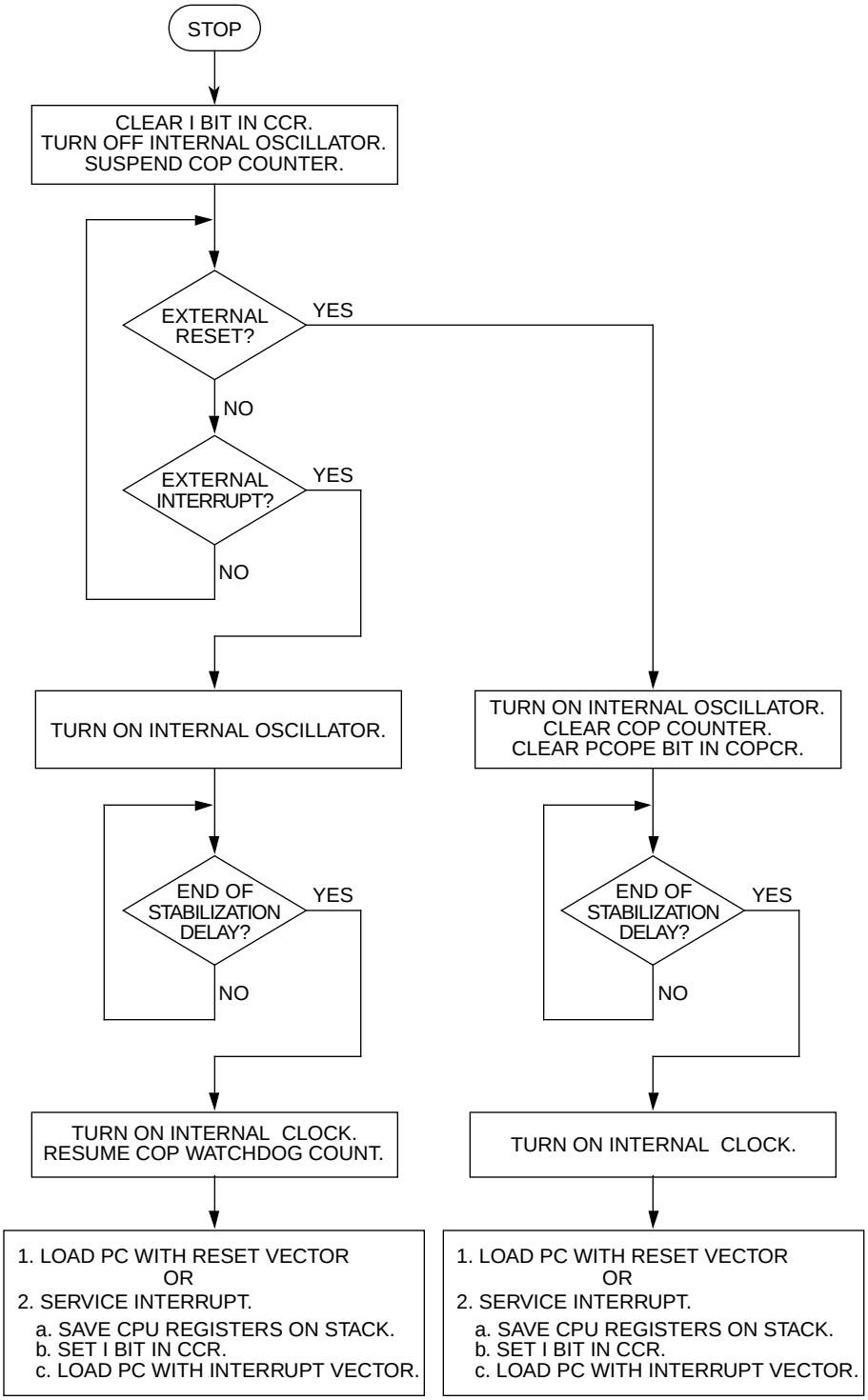


Figure B-8. Programmable COP Watchdog in STOP Mode (PCOPE = 1)

B.5.2 Non-Programmable COP Watchdog

A timeout of the 18-stage ripple counter in the non-programmable COP watchdog generates a reset. The timeout period is 64 ms when f_{OSC} = 4 MHz. Two memory locations control operation of the non-programmable COP watchdog:

- The non-programmable COP enable bit (NCOPE) in mask option register 2 (MOR2) — Programming the NCOPE bit in MOR2 to a logic one enables the non-programmable COP watchdog.

NOTE

Writing a logic one to the programmable COP enable bit (PCOPE) in the COP control register enables the programmable COP watchdog. Setting the PCOPE bit while the NCOPE bit is programmed to logic one enables both COP watchdogs to operate at the same time.

- The COP clear bit (COPC) at address $1FF0 — To clear the non-programmable COP watchdog and start a new COP timeout period, write a logic zero to bit 0 of address $1FF0. Reading address $1FF0 returns the mask option register 1 (MOR1) data at that location. (See **Figure B-1. Mask Option Register 1 (MOR1)**.)

B.5.2.1 Non-Programmable COP Watchdog in WAIT Mode

The non-programmable COP watchdog is active during WAIT mode. Software must periodically bring the MCU out of WAIT mode to clear the non-programmable COP watchdog.

B.5.2.2 Non-Programmable COP Watchdog in STOP Mode

The STOP instruction has the following effects on the non-programmable COP watchdog:

- Turns off the oscillator and turns off the COP watchdog counter
- Clears the COP watchdog counter

If the $\overline{\text{RESET}}$ pin brings the MCU out of STOP mode, the COP watchdog begins counting immediately. The reset function clears the COP counter again after the 4064-t_{CYC} clock stabilization delay.

If the $\overline{\text{IRQ}}$ pin brings the MCU out of STOP mode, the COP watchdog begins counting immediately. The IRQ function does not clear the COP counter again after the 4064-t_{CYC} clock stabilization delay. See Figure B-9.

NOTE

If the clock monitor is enabled (CME = 1), the STOP instruction causes it to time out and reset the MCU.

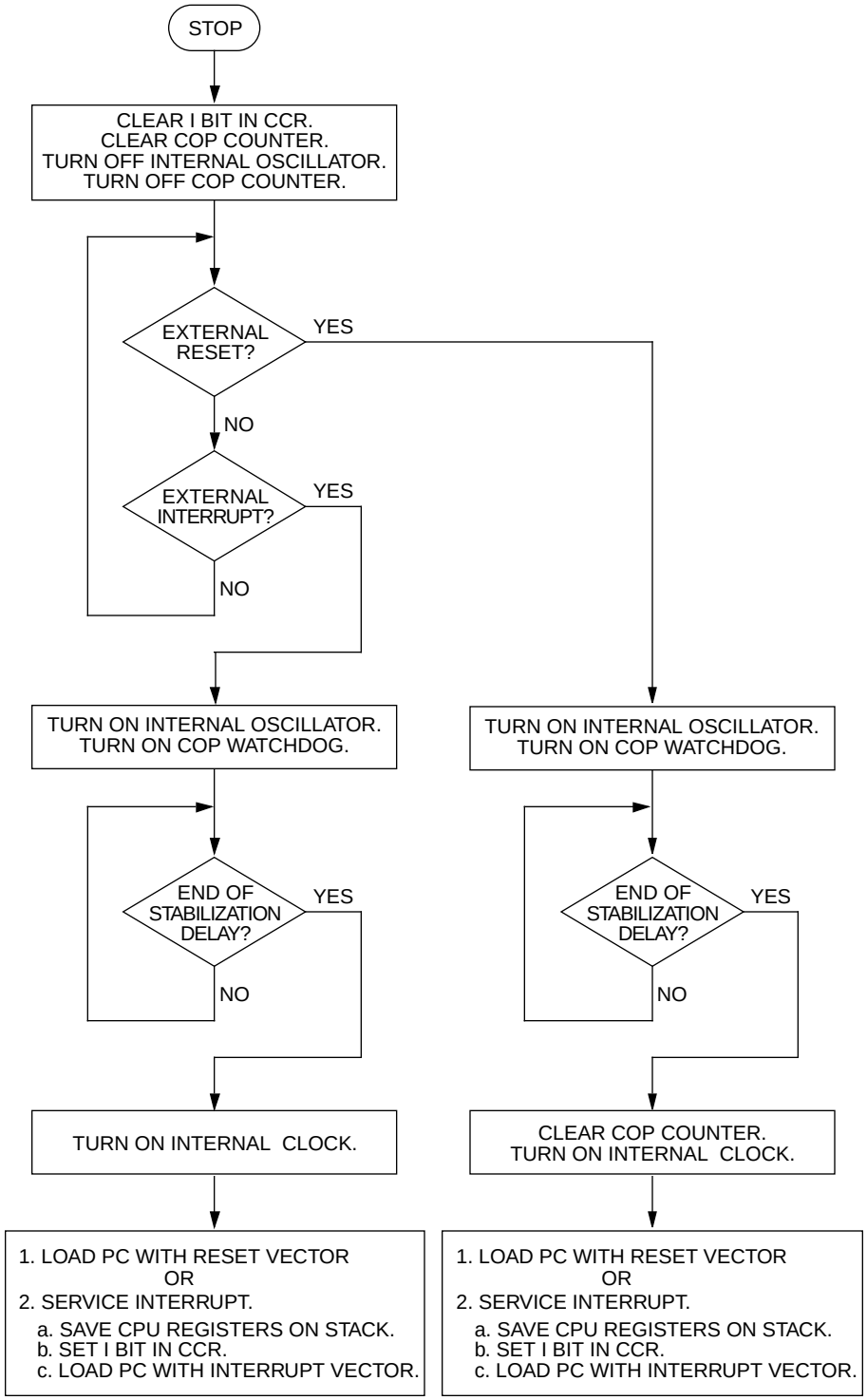


Figure B-9. Non-Programmable COP Watchdog in STOP Mode (NCOPE = 1)

B.6 DC ELECTRICAL CHARACTERISTICS

Table B-2. DC Electrical Characteristics (V_{DD} = 5.0 V ± 10%)

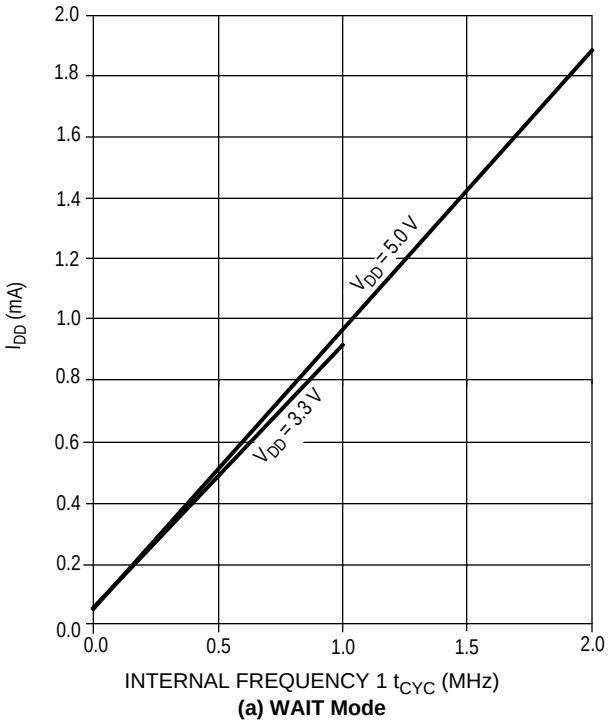
Characteristic	Symbol	Min	Typ(1)	Max	Unit
Output High Voltage					
I_{LOAD} = –0.8 mA					
PA7–PA0, PB7–PB0, PC6–PC0, TCMP	V_{OH}	V_{DD} – 0.8	—	—	V
I_{LOAD} = –1.6 mA					
PD4–PD1		V_{DD} – 0.8	—	—	V
I_{LOAD} –5.0 mA					
PC7		V_{DD} – 0.8	—	—	V
Output Low Voltage					
I_{LOAD} = 1.6 mA					
PA7–PA0, PB7–PB0, PC6–PC0, PD4–PD1	V_{OL}	—	—	0.4	V
I_{LOAD} = 20 mA					
PC7		—	—	0.4	V
Supply Current(2)					
Run(3)		—	2.78	7.0	mA
WAIT(4)		—	1.86	3.0	mA
STOP(5)	I_{DD}				
25 °C		—	5.0	50	µA
–40 °C to +85 °C		—	5.0	50	µA

1. Typical values reflect average measurements at midpoint of voltage range at 25 °C.
2. I_{DD} measured with port B pullup devices disabled.
3. Run (operating) I_{DD} measured using external square wave clock source (f_{OSC} = 4.2 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2.
4. WAIT I_{DD} measured using external square wave clock source (f_{OSC} = 4.2 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2. V_{IL} = 0.2 V, V_{IH} = V_{DD} – 0.2 V. All ports configured as inputs. SPI and SCI disabled. If SPI and SCI enabled, add 10% current draw. OSC2 capacitance linearly affects WAIT I_{DD}.
5. STOP I_{DD} measured with OSC1 = V_{DD}. All ports configured as inputs. V_{IL} = 0.2 V, V_{IH} = V_{DD} – 0.2 V.

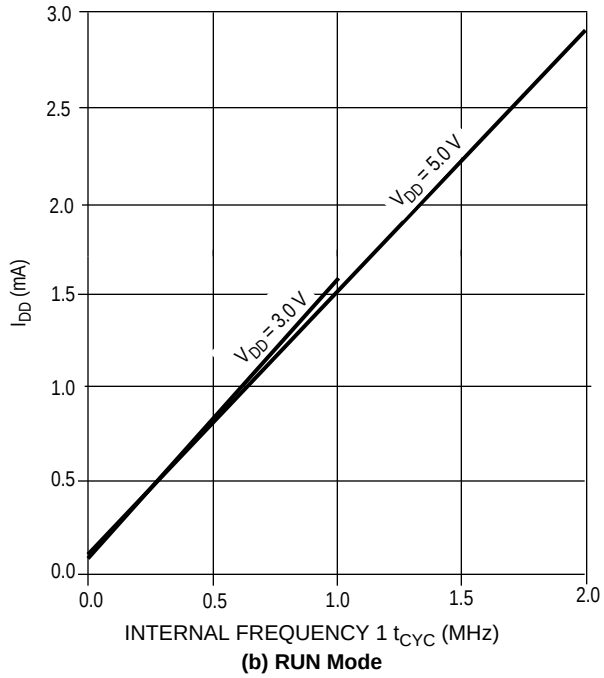
Table B-3. DC Electrical Characteristics (V_{DD} = 3.3 V ± 10%)

Characteristic	Symbol	Min	Typ(1)	Max	Unit
Output High Voltage I_{LOAD} = –0.2 mA PA7–PA0, PB7–PB0, PC6–PC0, TCMP I_{LOAD} = –0.4 mA PD4–PD1 I_{LOAD} = –1.5 mA PC7	V_{OH}	 V_{DD} – 0.3 V_{DD} – 0.3 V_{DD} – 0.3	 — — —	 — — —	 V V V
Output Low Voltage I_{LOAD} = 0.4 mA PA7–PA0, PB7–PB0, PC6–PC0, PD4–PD1 I_{LOAD} = 6.0 mA PC7	V_{OL}	 — —	 — —	 0.3 0.3	 V V
Supply Current Run(2) WAIT(3) STOP(4)	I_{DD}	 — — —	 1.51 0.972 2.0	 3.0 1.0 20	 mA mA µA

1. Typical values reflect average measurements at midpoint of voltage range at 25 °C.
2. Run (operating) I_{DD} measured using external square wave clock source (f_{OSC} = 2.0 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2.
3. WAIT I_{DD} measured using external square wave clock source (f_{OSC} = 2.0 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2. V_{IL} = 0.2 V, V_{IH} = V_{DD} – 0.2 V. All ports configured as inputs. SPI and SCI disabled. If SPI and SCI enabled, add 10% current draw. OSC2 capacitance linearly affects WAIT I_{DD}.
4. STOP I_{DD} measured with OSC1 = V_{DD}. All ports configured as inputs. V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V.



(a) WAIT Mode



(b) RUN Mode

Figure B-10. Typical Current vs. Internal Frequency for RUN and WAIT Modes

Table B-4. SPI Timing (V_{DD} = 4.5 Vdc–5.5 Vdc)

Number[1]	Characteristic	Symbol	Min	Max	Unit
	Operating Frequency Master Slave	 $f_{OP(M)}$ $f_{OP(S)}$	 dc dc	 0.5 2.1	 f_{OP} MHz
①	Cycle Time Master Slave	 $t_{CYC(M)}$ $t_{CYC(S)}$	 2.0 480	 — —	 t_{CYC} ns
②	Enable Lead Time Master Slave	 $t_{LEAD(M)}$ $t_{LEAD(S)}$	 (2) 240	 — —	 ns
③	Enable Lag Time Master Slave	 $t_{LAG(M)}$ $t_{LAG(S)}$	 (2) 720	 — —	 ns
④	Clock (SCK) High Time Master Slave	 $t_{W(SCKH)M}$ $t_{W(SCKH)S}$	 340 190	 — —	 ns ns
⑤	Clock (SCK) Low Time Master Slave	 $t_{W(SCKL)M}$ $t_{W(SCKL)S}$	 340 190	 — —	 ns ns
⑥	Data Setup Time (Inputs) Master Slave	 $t_{SU(M)}$ $t_{SU(S)}$	 100 100	 — —	 ns ns
⑦	Data Hold Time (Inputs) Master Slave	 $t_{H(M)}$ $t_{H(S)}$	 100 100	 — —	 ns ns
⑧	Access Time[3] Slave	t_A	0	120	ns
⑨	Disable Time[4] Slave	t_{DIS}	—	240	ns
⑩	Data Valid Time Master (Before Capture Edge) Slave (After Enable Edge)[5]	 $t_{V(M)}$ $t_{V(S)}$	 0.25 —	 — 240	 $t_{CYC(M)}$ ns
⑪	Data Hold Time (Outputs) Master (After Capture Edge) Slave (After Enable Edge)	 $t_{HO(M)}$ $t_{HO(S)}$	 0.25 0	 — —	 $t_{CYC(M)}$ ns
⑫	Rise Time[6] SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	 $t_{R(M)}$ $t_{R(S)}$	 — —	 100 2.0	 ns µs
⑬	Fall Time[7] SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	 $t_{F(M)}$ $t_{F(S)}$	 — —	 100 2.0	 ns µs

1. Numbers refer to dimensions in Figure 8-7 of *MC68HC705C8 Technical Data*, REV. 1.
2. Signal production depends on software.
3. Time to data active from high-impedance state.
4. Hold time to high-impedance state.
5. With 200 pF on all SPI pins.
6. 20% of V_{DD} to 70% of V_{DD}; C_L = 200 pF.
7. 70% of V_{DD} to 20% of V_{DD}; C_L = 200 pF.

Table B-5. SPI Timing (V_{DD} = 3.0 Vdc–3.6 Vdc)

Number[1]	Characteristic	Symbol	Min	Max	Unit
	Operating Frequency Master Slave	 $f_{OP(M)}$ $f_{OP(S)}$	 dc dc	 0.5 2.1	f_{OP} MHz
1	Cycle Time Master Slave	 $t_{CYC(M)}$ $t_{CYC(S)}$	 2.0 1	 — —	t_{CYC} µs
2	Enable Lead Time Master Slave	 $t_{LEAD(M)}$ $t_{LEAD(S)}$	 [2] 500	 — —	 ns
3	Enable Lag Time Master Slave	 $t_{LAG(M)}$ $t_{LAG(S)}$	 [2] 1500	 — —	 ns
4	Clock (SCK) High Time Master Slave	 $t_{W(SCKH)M}$ $t_{W(SCKH)S}$	 720 400	 — —	 ns ns
5	Clock (SCK) Low Time Master Slave	 $t_{W(SCKL)M}$ $t_{W(SCKL)S}$	 720 400	 — —	 ns ns
6	Data Setup Time (Inputs) Master Slave	 $t_{SU(M)}$ $t_{SU(S)}$	 200 200	 — —	 ns ns
7	Data Hold Time (Inputs) Master Slave	 $t_{H(M)}$ $t_{H(S)}$	 200 200	 — —	 ns ns
8	Access Time[3] Slave	t_A	0	250	ns
9	Disable Time[4] Slave	t_{DIS}	—	500	ns
10	Data Valid Time Master (Before Capture Edge) Slave (After Enable Edge)[5]	 $t_{V(M)}$ $t_{V(S)}$	 0.25 —	 — 500	 $t_{CYC(M)}$ ns
11	Data Hold Time (Outputs) Master (After Capture Edge) Slave (After Enable Edge)	 $t_{HO(M)}$ $t_{HO(S)}$	 0.25 0	 — —	 $t_{CYC(M)}$ ns
12	Rise Time[6] SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	 $t_{R(M)}$ $t_{R(S)}$	 — —	 200 2.0	 ns µs
13	Fall Time[7] SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	 $t_{F(M)}$ $t_{F(S)}$	 — —	 200 2.0	 ns µs

1. Numbers refer to dimensions in Figure 8-7 of *MC68HC705C8 Technical Data*, REV. 1.
2. Signal production depends on software.
3. Time to data active from high-impedance state.
4. Hold time to high-impedance state.
5. With 200 pF on all SPI pins.
6. 20% of V_{DD} to 70% of V_{DD}; C_L = 200 pF.
7. 70% of V_{DD} to 20% of V_{DD}; C_L = 200 pF.

B.7 ORDERING INFORMATION

Table B-6 provides ordering information for the MC68HC705C8A.

Table B-6. MC68HC705C8A Order Numbers

Package Type	Temperature Range	Order Number
40-Pin Plastic Dual In-Line Package (DIP)	0 °C to +70 °C –40 °C to +85 °C	MC68HC705C8AP(1) MC68HC705C8AC(2)P
44-Lead Plastic-Leaded Chip Carrier (PLCC)	0 °C to +70 °C –40 °C to +85 °C	MC68HC705C8AFN(3) MC68HC705C8ACFN
40-Pin Windowed Ceramic DIP (CERDIP)	0 °C to +70 °C –40 °C to +85 °C	MC68HC705C8AS(4) MC68HC705C8ACS
44-Lead Quad Flat Pack (QFP)	0 °C to +70 °C –40 °C to +85 °C	MC68HC705C8AFB(5) MC68HC705C8ACFB
42-Pin Shrink Dual In-Line Package (SDIP)	0 °C to +70 °C –40 °C to +85 °C	MC68HC705C8AB(6) MC68HC705C8ACB

1. P = Plastic dual in-line package (DIP).
2. C = Extended temperature range (–40 °C to +85 °C).
3. FN = Plastic-leaded chip carrier (PLCC).
4. S = Windowed ceramic DIP (CERDIP).
5. FB = 10 mm × 10 mm quad flat pack (QFP).
6. B = Shrink dual in-line plastic (SDIP).

B.8 PIN ASSIGNMENTS

B.8.1 DIP (MC68HC705C8AP)

MC68HC705C8AP pin assignments are identical to those of the MC68HC705C8P.

B.8.2 PLCC (MC68HC705C8AFN)

MC68HC705C8AFN pin assignments are identical to those of the MC68HC705C8FN.

B.8.3 CERDIP (MC68HC705C8AS)

MC68HC705C8AS pin assignments are identical to those of the MC68HC705C8S.

B.8.4 QFP (MC68HC705C8AFB)

MC68HC705C8AFB pin assignments, shown in Figure B-11, are identical to those of the MC68HC705C8FB.

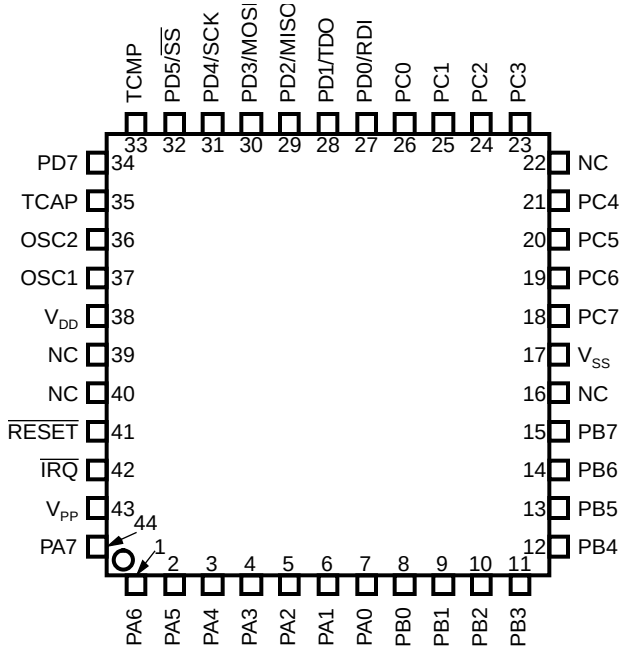


Figure B-11. MC68HC705C8AFB Pin Assignments

B.8.5 SDIP (MC68HC705C8AB)

MC68HC705C8AB pin assignments, shown in Figure B-12, are identical to those of the MC68HC705C8B.

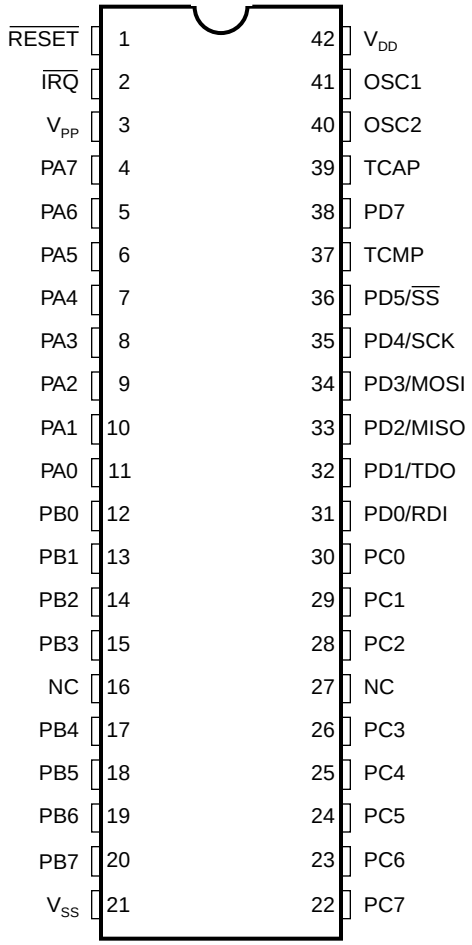


Figure B-12. MC68HC705C8AB Pin Assignments

B.9 PACKAGE DIMENSIONS

B.9.1 DIP (MC68HC705C8AP)

MC68HC705C8AP dimensions are identical to those of the MC68HC705C8P.

B.9.2 PLCC (MC68HC705C8AFN)

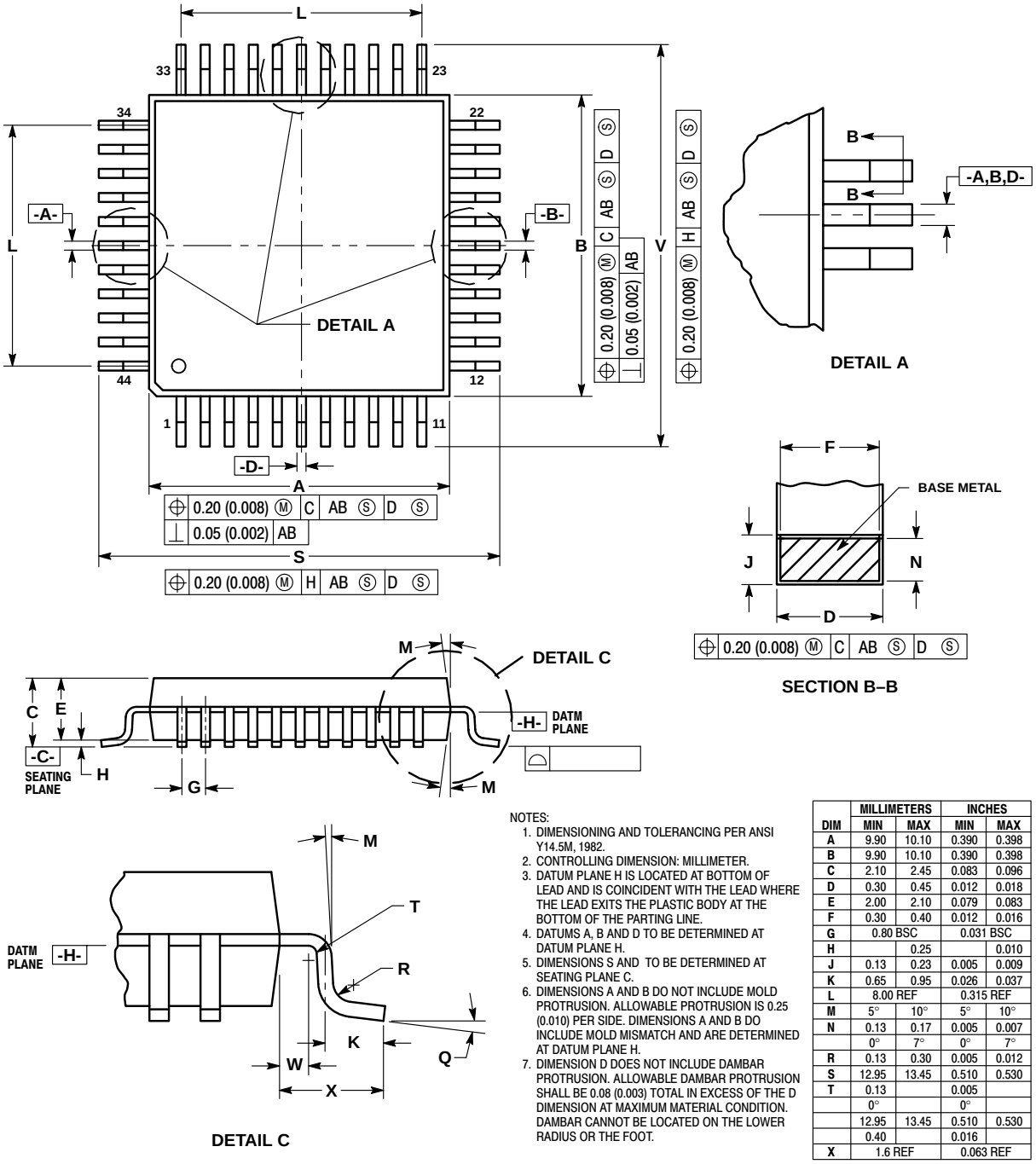
MC68HC705C8AFN dimensions are identical to those of the MC68HC705C8FN.

B.9.3 CERDIP (MC68HC705C8AS)

MC68HC705C8AS dimensions are identical to those of the MC68HC705C8S.

B.9.4 QFP (MC68HC705C8AFB)

MC68HC705C8AFB dimensions, shown in Figure B-13, are identical to those of the MC68HC705C8FB.



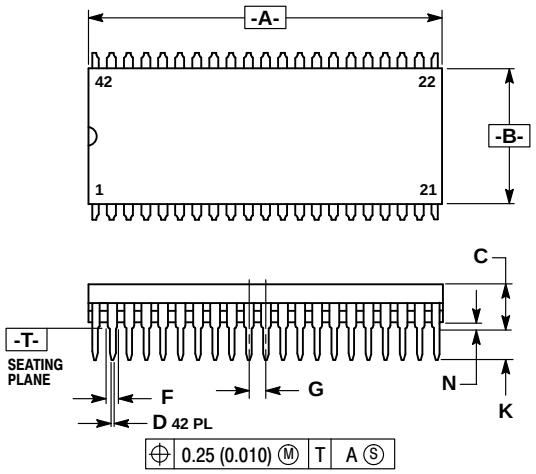
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS S AND TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.30	0.45	0.012	0.018
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
H		0.25		0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	8.00 REF		0.315 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13		0.005	
	0°		0°	
	12.95	13.45	0.510	0.530
	0.40		0.016	
X	1.6 REF		0.063 REF	

Figure B-13. MC68HC705C8AFB Package Dimensions

B.9.5 SDIP (MC68HC705C8AB)

MC68HC705C8AB dimensions, shown in Figure B-14, are identical to those of the MC68HC705C8B.



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.032	0.046	0.81	1.17
G	0.070 BSC		1.778 BSC	
H	0.300 BSC		7.62 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

Figure B-14. MC68HC705C8AB Package Dimensions

APPENDIX C
MC68HSC705C8A

The MC68HSC705C8A is an enhanced, high-speed version of the MC68HC705C8. Features of the MC68HSC705C8A include:

- 4-MHz bus speed
- Mask option registers that control the following:
  - Enabling of port B external interrupt capability
  - Selection of programmable and/or non-programmable COP watchdogs
- High current drive on pin C7

The data in *MC68HC705C8 Technical Data,* REV. 1 applies to the MC68HSC705C8A with the exceptions given in this appendix.

C.1 MEMORY MAP

Figure C-2 is a memory map of the MC68HSC705C8A.

C.2 MASK OPTION REGISTER 1 (MOR1)

MOR1 is an EPROM register that enables the port B pullup devices. Data from MOR1 is latched on the rising edge of the voltage on the $\overline{\text{RESET}}$ pin.

		7	6	5	4	3	2	1	0
MOR1 $1FF0	READ: / WRITE:	PBPU7	PBPU6	PBPU5	PBPU4	PBPU3	PBPU2	PBPU1	PBPU0/ COPC
	RESET:	UNAFFECTED BY RESET							
	ERASED:	0	0	0	0	0	0	0	0

Figure C-1. Mask Option Register 1 (MOR1)

PBPU7–PBPU0 — Port B Pullup Bits 7–0
These EPROM bits enable the port B pullup devices.
1 = Port B pullups enabled
0 = Port B pullups disabled

NOTE

When using the MC68HSC705C8A in an MC68HC705C8 or MC68HSC705C8 application, program locations $1FF0 and $1FF1 to $00.

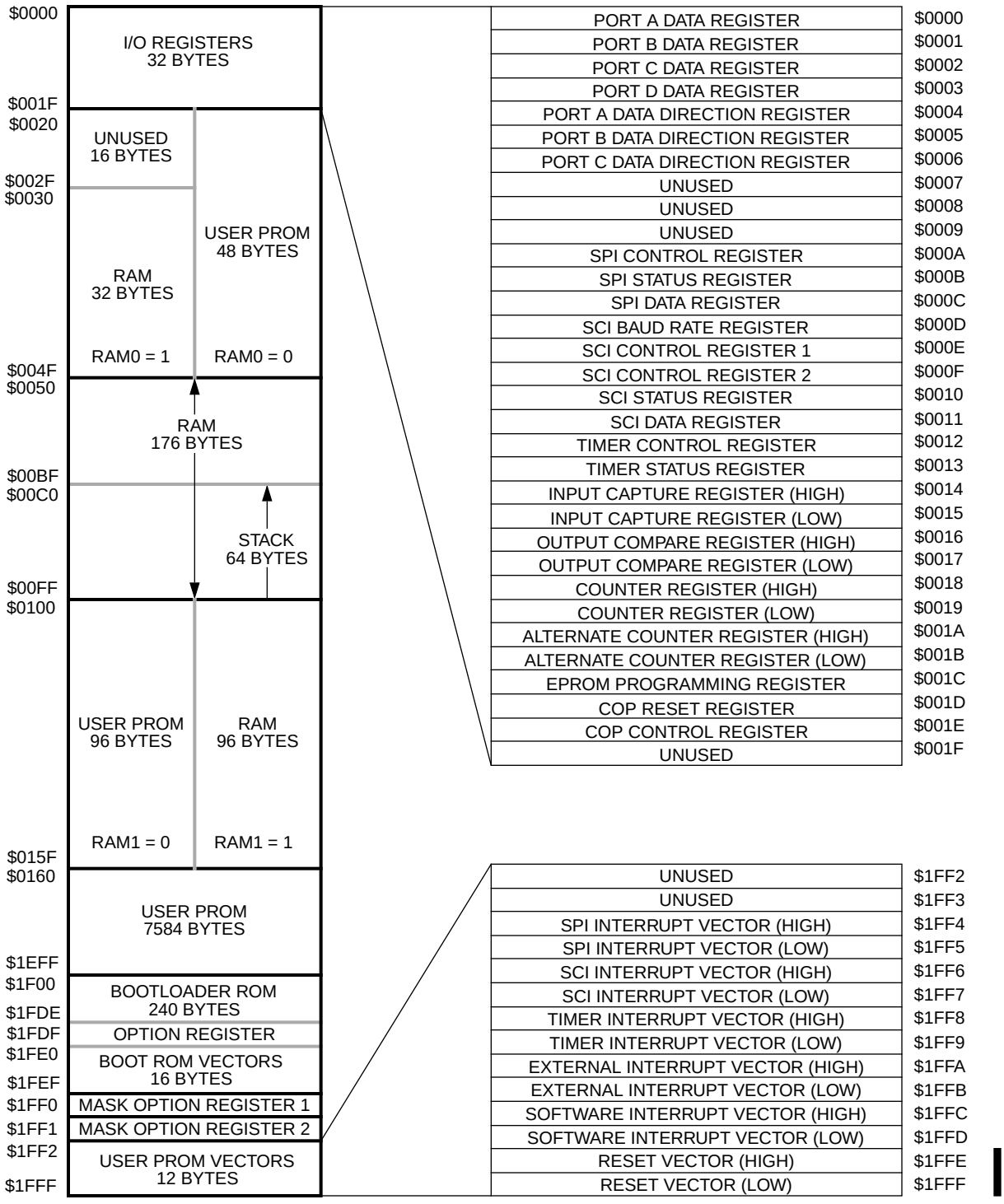


Figure C-2. MC68HSC705C8A Memory Map

C.3 MASK OPTION REGISTER 2 (MOR2)

MOR2 is an EPROM register that enables the non-programmable COP watchdog. Data from MOR2 is latched on the rising edge of the voltage on the $\overline{\text{RESET}}$ pin.

		7	6	5	4	3	2	1	0
MOR2 $1FF1	READ:	—	—	—	—	—	—	—	NCOPE
	WRITE:								
	RESET:	UNAFFECTED BY RESET							
	ERASED:	0	0	0	0	0	0	0	0

Figure C-3. Mask Option Register 2 (MOR2)

NCOPE — Non-Programmable COP Watchdog Enable

This EPROM bit enables the non-programmable COP watchdog.

1 = Non-programmable COP watchdog enabled

0 = Non-programmable COP watchdog disabled

C.4 PORT B EXTERNAL INTERRUPTS

When the following three conditions are true, a port B pin (PBx) acts as an external interrupt pin:

- The corresponding port B pullup bit (PBPUx) in MOR1 is programmed to a logic one.
- The corresponding port B data direction bit (DDRBx) in data direction register B is a logic zero.
- The clear interrupt mask instruction (CLI) has cleared the I bit in the condition code register.

The Port B external interrupt pins can be negative edge-sensitive only or both negative edge- and low level-sensitive, depending on the state of the IRQ bit in the option register (OPTION at location $1FDF). When the IRQ bit is a logic one:

- A falling edge or a low level on a port B external interrupt pin latches an external interrupt request.
- As long as any port B external interrupt pin is low, an external interrupt request is present, and the CPU continues to execute the interrupt service routine.

When the IRQ bit is a logic zero:

- A falling edge on a port B external interrupt pin latches an external interrupt request.
- A subsequent port B external interrupt request can be latched only after the voltage level of the previous port B external interrupt signal returns to a logic one and then falls again to a logic zero. Figure C-4 shows the port B I/O logic.

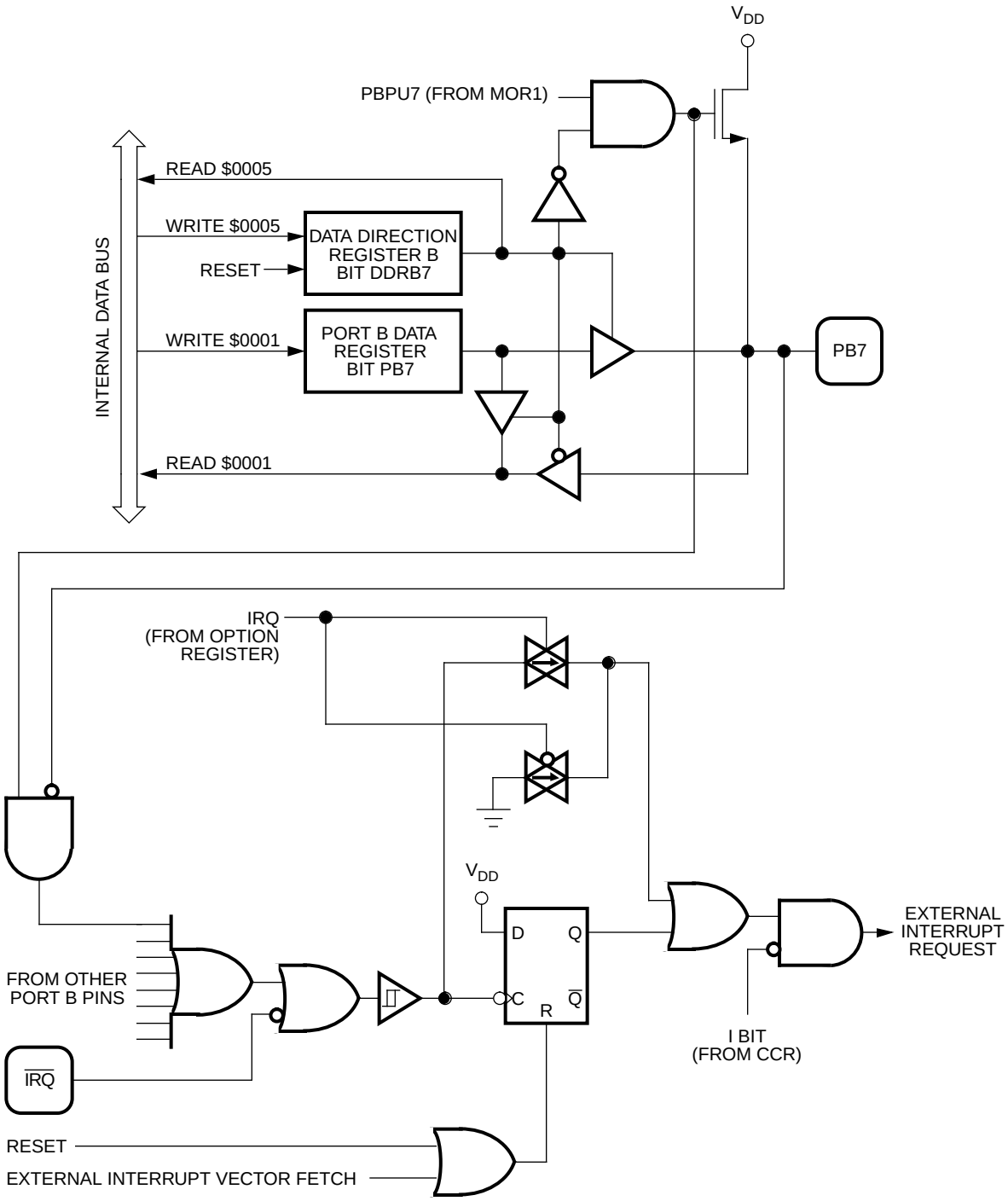


Figure C-4. Port B I/O Logic

C.5 COP WATCHDOG SELECTION

For COP watchdog application compatibility with devices such as the MC68HC705C8 and MC68HC05C4A, the MC68HSC705C8A has two different COP watchdogs. One COP watchdog has four programmable timeout periods, and the other has one fixed, non-programmable timeout period. Figure C-5 is a block diagram of the two COP watchdogs.

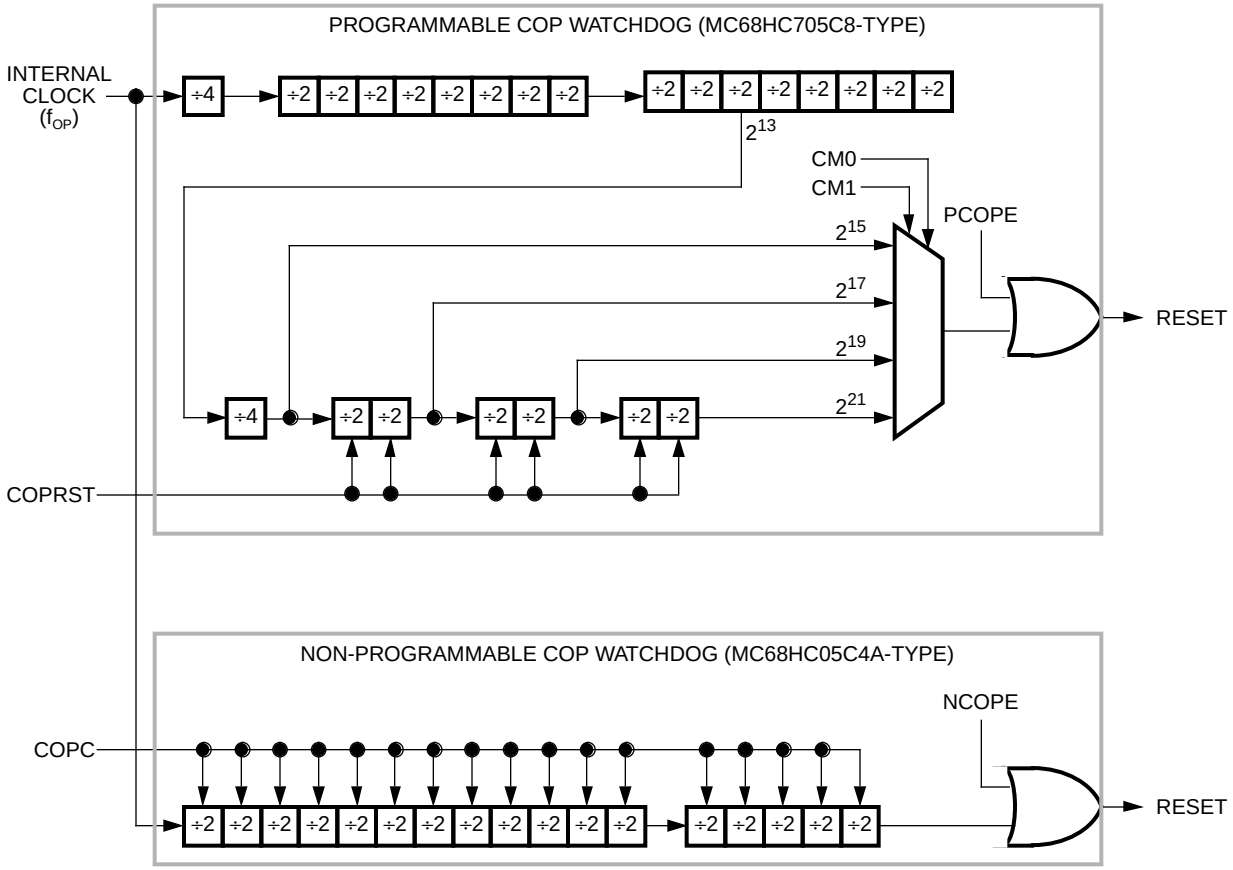


Figure C-5. MC68HSC705C8A COP Watchdogs

C.5.1 Programmable COP Watchdog

A timeout of the 18-stage ripple counter in the programmable COP watchdog generates a reset. Two registers control and monitor operation of the programmable COP watchdog:

- COP reset register
- COP control register

C.5.1.1 COP Reset Register (COPRST)

To clear the programmable COP watchdog and begin a new timeout period, write the following values to the COP reset register:

1. $55
2. $AA

The $55 write must precede the $AA write. Instructions may be executed between the write operations provided that the COP watchdog does not time out before the second write.

		7	6	5	4	3	2	1	0
COPRST $001D	READ:								
	WRITE:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RESET:	X	X	X	X	X	X	X	X

X = INDETERMINATE

Figure C-6. COP Reset Register (COPRST)

C.5.1.2 COP Control Register (COPCR)

The COP control register does the following:

- Flags programmable COP watchdog resets
- Enables the clock monitor
- Enables the programmable COP watchdog
- Controls the timeout period of the programmable COP watchdog

		7	6	5	4	3	2	1	0
COPCR $001E	READ:	0	0	0	COPF	CME	PCOPE	CM1	CM0
	WRITE:								
	RESET:	0	0	0	U	0	0	0	0

U = UNAFFECTED

Figure C-7. COP Control Register (COPCR)

BITS 7–5 — Unused

Bits 7–5 always read as logic zeros. Reset clears bits 7–5.

COPF — COP Flag

This read-only bit is set when a timeout of the programmable COP watchdog occurs or when the clock monitor detects a slow or absent internal clock. Clear the COPF bit by reading the COP control register. Reset has no effect on the COPF bit.

1 = COP timeout or internal clock failure
0 = No COP timeout and no internal clock failure

CME — Clock Monitor Enable

This read/write bit enables the clock monitor. The clock monitor sets the COPF bit and generates a reset if it detects an absent internal clock for a period of from 5 μs to 100 μs. The CME bit is readable at any time but can be written only once after reset. Reset clears the CME bit.

1 = Clock monitor enabled
0 = Clock monitor disabled

NOTE

Do not enable the clock monitor in applications with an internal clock frequency of 200 kHz or less.

If the clock monitor detects a slow clock, it drives the bidirectional $\overline{\text{RESET}}$ pin low for four clock cycles. If the clock monitor detects an absent clock, it drives the $\overline{\text{RESET}}$ pin low until the clock recovers.

PCOPE — Programmable COP Watchdog Enable

This read/write bit enables the programmable COP watchdog. PCOPE is readable at any time but can be written only once after reset. Reset clears the PCOPE bit.

1 = Programmable COP watchdog enabled
0 = Programmable COP watchdog disabled

NOTE

Programming the non-programmable COP enable bit (NCOPE) in mask option register 2 (MOR2) to logic one enables the non-programmable COP watchdog. Setting the PCOPE bit while the NCOPE bit is programmed to logic one enables both COP watchdogs to operate at the same time.

CM1 and CM0 — COP Mode Bits

These read/write bits select the timeout period of the programmable COP watchdog as shown in Table B-1. CM1 and CM0 can be cleared only by reset. Reset clears the CM1 and CM0 bits.

Table C-1. Programmable COP Timeout Period Selection

CM1:CM0	COP Timeout Rate	Programmable COP Timeout Period			
		f_{OSC} = 8.0 MHz f_{OP} = 4.0 MHz	f_{OSC} = 4.0 MHz f_{OP} = 2.0 MHz	f_{OSC} = 3.5795 MHz f_{OP} = 1.7897 MHz	f_{OSC} = 2.0 MHz f_{OP} = 1.0 MHz
00	$f_{OP} \div 2^{15}$	8.192 ms	16.38 ms	18.31 ms	32.77 ms
01	$f_{OP} \div 2^{17}$	32.77 ms	65.54 ms	73.24 ms	131.07 ms
10	$f_{OP} \div 2^{19}$	131.07 ms	262.14 ms	292.95 ms	524.29 ms
11	$f_{OP} \div 2^{21}$	524.29 ms	1.048 s	1.172 s	2.097 s

C.5.1.3 Programmable COP Watchdog in WAIT Mode

The programmable COP watchdog is active during WAIT mode. Software must periodically bring the MCU out of WAIT mode to clear the programmable COP watchdog.

C.5.1.4 Programmable COP Watchdog in STOP Mode

The STOP instruction turns off the internal oscillator and suspends the COP watchdog counter. If the $\overline{\text{RESET}}$ pin brings the MCU out of STOP mode, the reset function clears and disables the COP watchdog.

If the $\overline{\text{IRQ}}$ pin brings the MCU out of STOP mode, the COP counter resumes counting from its suspended value after the 4064-t_{CYC} clock stabilization delay. See Figure C-8.

NOTE

If the clock monitor is enabled (CME = 1), the STOP instruction causes it to time out and reset the MCU.

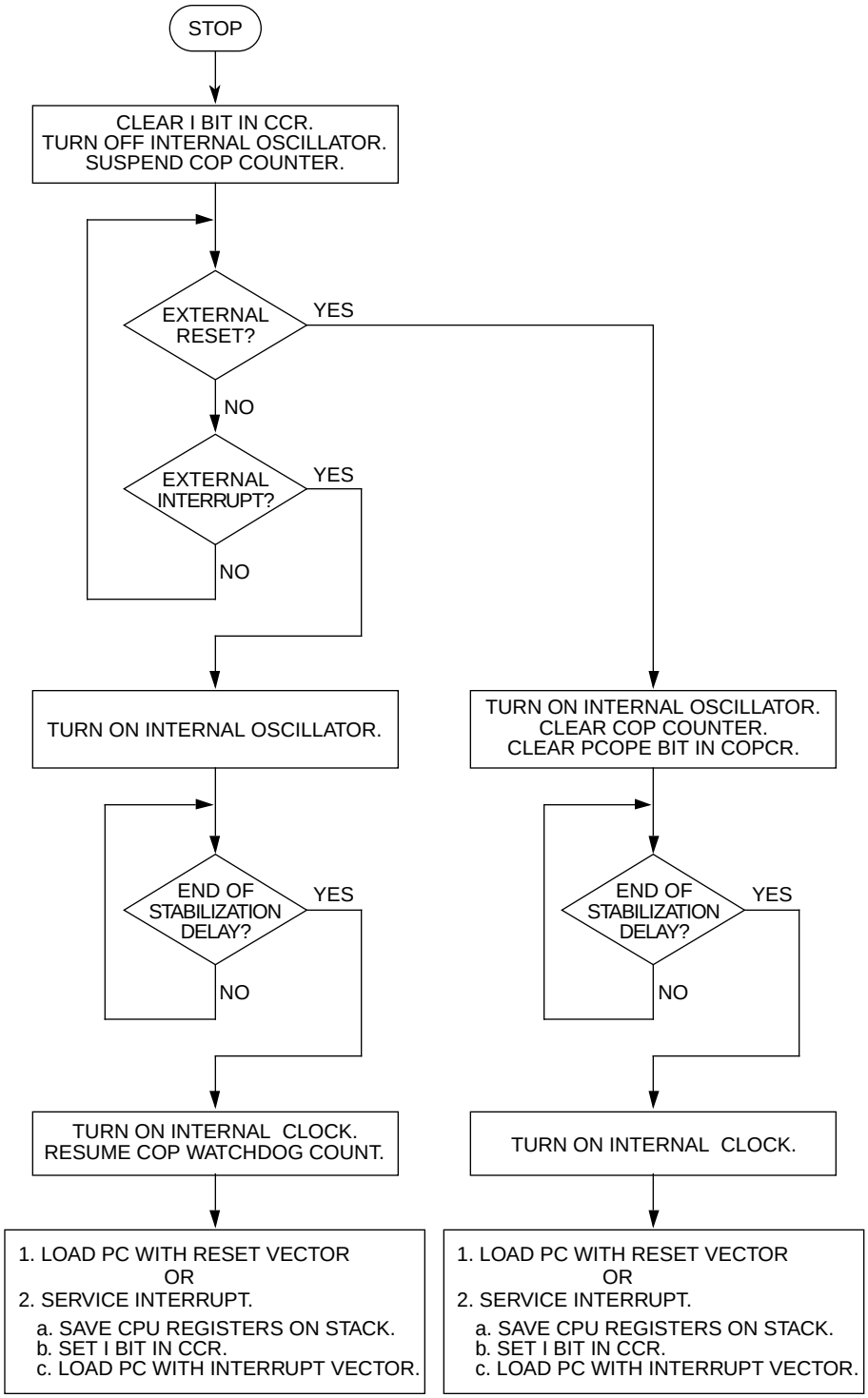


Figure C-8. Programmable COP Watchdog in STOP Mode (PCOPE = 1)

C.5.2 Non-Programmable COP Watchdog

A timeout of the 18-stage ripple counter in the non-programmable COP watchdog generates a reset. The timeout period is 64 ms when f_{OSC} = 4 MHz. Two memory locations control operation of the non-programmable COP watchdog:

- The non-programmable COP enable bit (NCOPE) in mask option register 2 (MOR2) — Programming the NCOPE bit in MOR2 to a logic one enables the non-programmable COP watchdog.

NOTE

Writing a logic one to the programmable COP enable bit (PCOPE) in the COP control register enables the programmable COP watchdog. Setting the PCOPE bit while the NCOPE bit is programmed to logic one enables both COP watchdogs to operate at the same time.

- The COP clear bit (COPC) at address $1FF0 — To clear the non-programmable COP watchdog and start a new COP timeout period, write a logic zero to bit 0 of address $1FF0. Reading address $1FF0 returns the mask option register 1 (MOR1) data at that location. (See **Figure C-1. Mask Option Register 1 (MOR1)**.)

C.5.2.1 Non-Programmable COP Watchdog in WAIT Mode

The non-programmable COP watchdog is active during WAIT mode. Software must periodically bring the MCU out of WAIT mode to clear the non-programmable COP watchdog.

C.5.2.2 Non-Programmable COP Watchdog in STOP Mode

The STOP instruction has the following effects on the non-programmable COP watchdog:

- Turns off the oscillator and turns off the COP watchdog counter
- Clears the COP watchdog counter

If the $\overline{\text{RESET}}$ pin brings the MCU out of STOP mode, the COP watchdog begins counting immediately. The reset function clears the COP counter again after the 4064-t_{CYC} clock stabilization delay.

If the $\overline{\text{IRQ}}$ pin brings the MCU out of STOP mode, the COP watchdog begins counting immediately. The IRQ function does not clear the COP counter again after the 4064-t_{CYC} clock stabilization delay. See Figure C-9.

NOTE

If the clock monitor is enabled (CME = 1), the STOP instruction causes it to time out and reset the MCU.

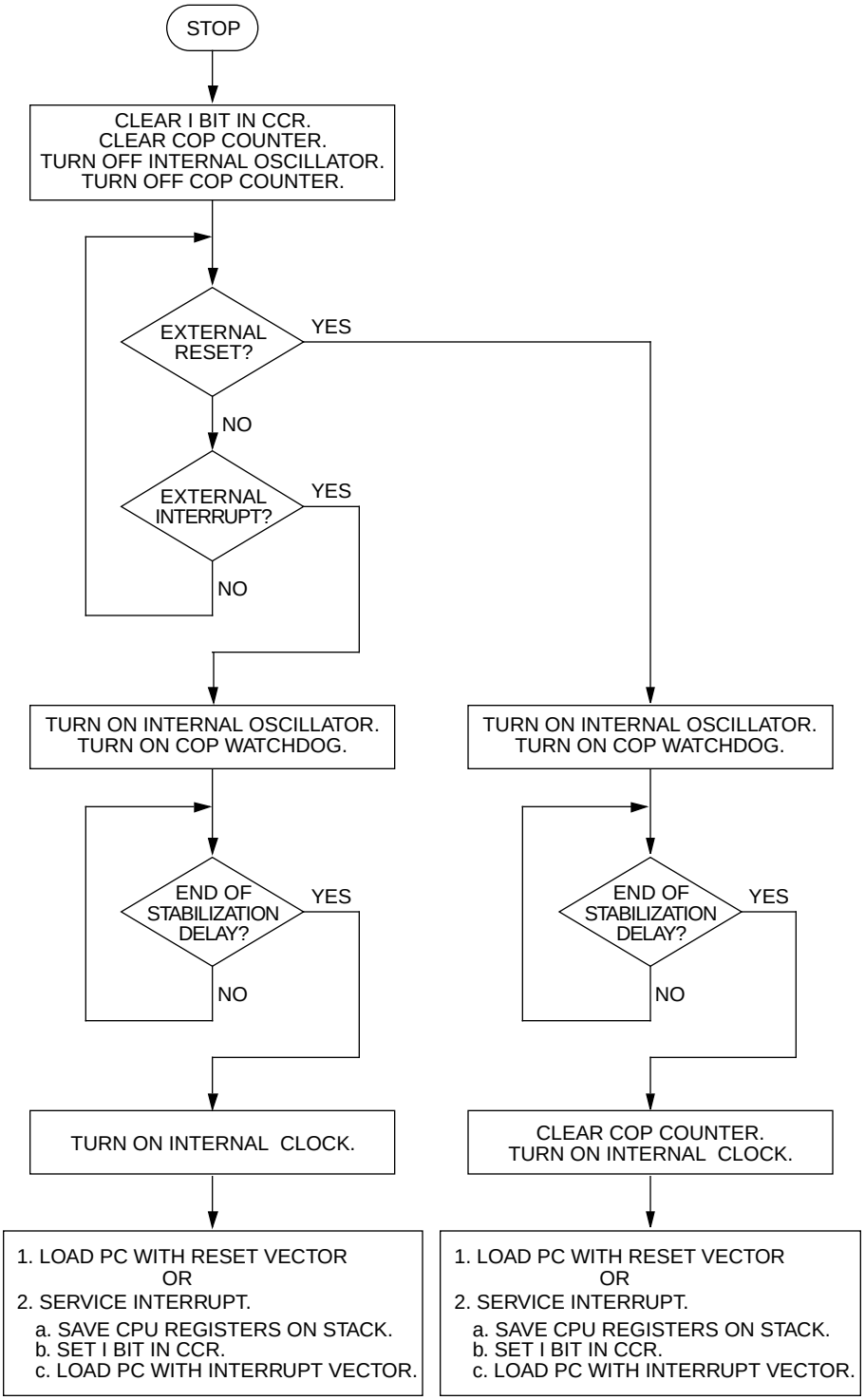


Figure C-9. Non-Programmable COP Watchdog in STOP Mode (NCOPE = 1)

C.6 DC ELECTRICAL CHARACTERISTICS

Table C-2. High-Speed DC Electrical Characteristics (V_{DD} = 5.0 V ± 10%)

Characteristic	Symbol	Min	Typ(1)	Max	Unit
Output High Voltage					
I_{LOAD} = –0.8 mA					
PA7–PA0, PB7–PB0, PC6–PC0, TCMP	V_{OH}	V_{DD} – 0.8	—	—	V
I_{LOAD} = –1.6 mA					
PD4–PD1		V_{DD} – 0.8	—	—	V
I_{LOAD} –5.0 mA					
PC7		V_{DD} – 0.8	—	—	V
Output Low Voltage					
I_{LOAD} = 1.6 mA					
PA7–PA0, PB7–PB0, PC6–PC0, PD4–PD1	V_{OL}	—	—	0.4	V
I_{LOAD} = 20 mA					
PC7		—	—	0.4	V
Supply Current(2)					
Run(3)	I_{DD}	—	7.30	14	mA
WAIT(4)		—	1.76	7.0	mA
STOP(5)					
25 °C		—	2.0	50	µA
–40 °C to +85 °C		—	2.0	50	µA

1. Typical values reflect average measurements at midpoint of voltage range at 25 °C.
2. I_{DD} measured with port B pullup devices disabled.
3. Run (operating) I_{DD} measured using external square wave clock source (f_{OSC} = 8.0 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2.
4. WAIT I_{DD} measured using external square wave clock source (f_{OSC} = 4.2 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2. V_{IL} = 0.2 V, V_{IH} = V_{DD} – 0.2 V. All ports configured as inputs. SPI and SCI disabled. If SPI and SCI enabled, add 10% current draw. OSC2 capacitance linearly affects WAIT I_{DD}.
5. STOP I_{DD} measured with OSC1 = V_{DD}. All ports configured as inputs. V_{IL} = 0.2 V, V_{IH} = V_{DD} – 0.2 V.

Table C-3. High-Speed DC Electrical Characteristics (V_{DD} = 3.3 V ± 10%)

Characteristic	Symbol	Min	Typ(1)	Max	Unit
Output High Voltage I_{LOAD} = –0.2 mA PA7–PA0, PB7–PB0, PC6–PC0, TCMP I_{LOAD} = –0.4 mA PD4–PD1 I_{LOAD} = –1.5 mA PC7	V_{OH}	 V_{DD} – 0.3 V_{DD} – 0.3 V_{DD} – 0.3	 — — —	 — — —	 V V V
Output Low Voltage I_{LOAD} = 0.4 mA PA7–PA0, PB7–PB0, PC6–PC0, PD4–PD1 I_{LOAD} = 6.0 mA PC7	V_{OL}	 — —	 — —	 0.3 0.3	 V V
Supply Current Run(2) WAIT(3) STOP(4)	I_{DD}	 — — —	 2.29 645 0.2	 6.0 2.0 20	 mA µA µA

1. Typical values reflect average measurements at midpoint of voltage range at 25 °C.
2. Run (operating) I_{DD} measured using external square wave clock source (f_{OSC} = 4.2 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2.
3. WAIT I_{DD} measured using external square wave clock source (f_{OSC} = 2.0 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20pF on OSC2. V_{IL} = 0.2 V, V_{IH} = V_{DD} – 0.2 V. All ports configured as inputs. SPI and SCI disabled. If SPI and SCI enabled, add 10% current draw. OSC2 capacitance linearly affects WAIT I_{DD}.
4. STOP I_{DD} measured with OSC1 = V_{DD}. All ports configured as inputs. V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V.

C.7 CONTROL TIMING

Table C-4. High-Speed Control Timing (V_{DD} = 5.0 V ± 10%)

Characteristic	Symbol	Min	Max	Unit
Oscillator Frequency Crystal Oscillator External Clock	f_{OSC}	— dc	8.0 8.0	MHz
Internal Operating Frequency ($f_{OSC} \div 2$) Crystal Oscillator External Clock	f_{OP}	— dc	4.0 4.0	MHz
Cycle Time	t_{CYC}	250	—	ns
Input Capture Pulse Width	t_{TH}, t_{TL}	65	—	ns
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}	65	—	ns
OSC1 Pulse Width	t_{OH}, t_{OL}	45	—	ns

Table C-5. High-Speed Control Timing (V_{DD} = 3.3 V ± 10%)

Characteristic	Symbol	Min	Max	Unit
Oscillator Frequency Crystal Oscillator External Clock	f_{OSC}	— dc	4.0 4.0	MHz
Internal Operating Frequency ($f_{OSC} \div 2$) Crystal Oscillator External Clock	f_{OP}	— dc	2.0 2.0	MHz
Cycle Time	t_{CYC}	476	—	ns
Input Capture Pulse Width	t_{TH}, t_{TL}	125	—	ns
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}	125	—	ns
OSC1 Pulse Width	t_{OH}, t_{OL}	90	—	ns

C.8 SERIAL PERIPHERAL INTERFACE (SPI) TIMING

Table C-6. High-Speed SPI Timing (V_{DD} = 5.0 V ± 10 %)

Diagram Number(1)	Characteristic	Symbol	Min	Max	Unit
	Operating Frequency Master Slave	 $f_{OP(S)}$ $f_{OP(S)}$	 dc dc	 0.5 4.0	f_{OP} MHz
①	Cycle Time Master Slave	 $t_{CYC(M)}$ $t_{CYC(S)}$	 2.0 250	 — —	t_{CYC} ns
②	Enable Lead Time Master Slave	 $t_{LEAD(M)}$ $t_{LEAD(S)}$	 NOTE (2) 125	 — —	 ns
③	Enable Lag Time Master Slave	 $t_{LAG(M)}$ $t_{LAG(S)}$	 NOTE(2) 375	 — —	 ns
④	Clock (SCK) High Time Master Slave	 $t_{W(SCKH)M}$ $t_{W(SCKH)S}$	 170 95	 — —	 ns ns
⑤	Clock (SCK) Low Time Master Slave	 $t_{W(SCKL)M}$ $t_{W(SCKL)S}$	 170 95	 — —	 ns ns
⑥	Data Setup Time (Inputs) Master Slave	 $t_{SU(M)}$ $t_{SU(S)}$	 50 50	 — —	 ns ns
⑦	Data Hold Time (Inputs) Master Slave	 $t_{H(M)}$ $t_{H(S)}$	 50 50	 — —	 ns ns
⑧	Access Time(3) Slave	 t_A	 0	 60	 ns
⑨	Disable Time(4) Slave	 t_{DIS}	 —	 120	 ns
⑩	Data Valid Time Master (Before Capture Edge) Slave (After Enable Edge)(5)	 $t_{V(M)}$ $t_{V(S)}$	 0.25 —	 — 120	 $t_{CYC(M)}$ ns
⑪	Data Hold Time (Outputs) Master (After Capture Edge) Slave (After Enable Edge)	 $t_{HO(M)}$ $t_{HO(S)}$	 0.25 0	 — —	 $t_{CYC(M)}$ ns
⑫	Rise Time(6) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	 t_{RM} t_{RS}	 — —	 50 2.0	 ns µs
⑬	Fall Time(7) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	 t_{FM} t_{FS}	 — —	 50 2.0	 ns µs

1. Diagram numbers refer to dimensions in Figure 8-7 in *MC68HC705C8 Technical Data,* REV. 1.
2. Signal production depends on software.
3. Time to data active from high-impedance state.
4. Hold time to high-impedance state.
5. With 200 pF on all SPI pins.
6. 20% of V_{DD} to 70% of V_{DD}; C_L = 200 pF.
7. 70% of V_{DD} to 20% of V_{DD}; C_L = 200 pF.

Table C-7. High-Speed SPI Timing (V_{DD} = 3.3 V ± 10%)

Diagram Number[1]	Characteristic	Symbol	Min	Max	Unit
	Operating Frequency Master Slave	 $f_{OP(S)}$ $f_{OP(S)}$	 dc dc	 0.5 2.1	f_{OP} MHz
①	Cycle Time Master Slave	 $t_{CYC(M)}$ $t_{CYC(S)}$	 2.0 480	 — —	t_{CYC} ns
②	Enable Lead Time Master Slave	 $t_{LEAD(M)}$ $t_{LEAD(S)}$	 NOTE [2] 240	 — —	 ns
③	Enable Lag Time Master Slave	 $t_{LAG(M)}$ $t_{LAG(S)}$	 NOTE[2] 720	 — —	 ns
④	Clock (SCK) High Time Master Slave	 $t_{W(SCKH)M}$ $t_{W(SCKH)S}$	 340 190	 — —	 ns ns
⑤	Clock (SCK) Low Time Master Slave	 $t_{W(SCKL)M}$ $t_{W(SCKL)S}$	 340 190	 — —	 ns ns
⑥	Data Setup Time (Inputs) Master Slave	 $t_{SU(M)}$ $t_{SU(S)}$	 100 100	 — —	 ns ns
⑦	Data Hold Time (Inputs) Master Slave	 $t_{H(M)}$ $t_{H(S)}$	 100 100	 — —	 ns ns
⑧	Access Time[3] Slave	 t_A	 0	 120	 ns
⑨	Disable Time[4] Slave	 t_{DIS}	 —	 240	 ns
⑩	Data Valid Time Master (Before Capture Edge) Slave (After Enable Edge)[5]	 $t_{V(M)}$ $t_{V(S)}$	 0.25 —	 — 240	 $t_{CYC(M)}$ ns
⑪	Data Hold Time (Outputs) Master (After Capture Edge) Slave (After Enable Edge)	 $t_{HO(M)}$ $t_{HO(S)}$	 0.25 0	 — —	 $t_{CYC(M)}$ ns
⑫	Rise Time[6] SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	 t_{RM} t_{RS}	 — —	 100 2.0	 ns µs
⑬	Fall Time[7] SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)	 t_{FM} t_{FS}	 — —	 100 2.0	 ns µs

1. Diagram numbers refer to dimensions in Figure 8-7 in *MC68HC705C8 Technical Data,* REV. 1.
2. Signal production depends on software.
3. Time to data active from high-impedance state.
4. Hold time to high-impedance state.
5. With 200 pF on all SPI pins.
6. 20% of V_{DD} to 70% of V_{DD}; C_L = 200 pF.
7. 70% of V_{DD} to 20% of V_{DD}; C_L = 200 pF.

C.9 ORDERING INFORMATION

Table B-6 provides ordering information for the MC68HSC705C8A.

Table C-8. MC68HSC705C8A Order Numbers

Package Type	Temperature Range	Order Number
40-Pin Plastic Dual In-Line Package (DIP)	0 °C to +70 °C –40 °C to +85 °C	MC68HSC705C8AP(1) MC68HSC705C8AC(2)P
44-Lead Plastic-Leaded Chip Carrier (PLCC)	0 °C to +70 °C –40 °C to +85 °C	MC68HSC705C8AFN(3) MC68HSC705C8ACFN
40-Pin Windowed Ceramic DIP (CERDIP)	0 °C to +70 °C –40 °C to +85 °C	MC68HSC705C8AS(4) MC68HSC705C8ACS
44-Lead Quad Flat Pack (QFP)	0 °C to +70 °C –40 °C to +85 °C	MC68HSC705C8AFB(5) MC68HSC705C8ACFB
42-Pin Shrink Dual In-Line Package (SDIP)	0 °C to +70 °C –40 °C to +85 °C	MC68HSC705C8AB(6) MC68HSC705C8ACB

1. P = Plastic dual in-line package (DIP).
2. C = Extended temperature range (–40 °C to +85 °C).
3. FN = Plastic-leaded chip carrier (PLCC).
4. S = Windowed ceramic DIP (CERDIP).
5. FB = 10 mm × 10 mm quad flat pack (QFP).
6. B = Shrink dual in-line plastic (SDIP).

C.10 PIN ASSIGNMENTS

C.10.1 DIP (MC68HSC705C8AP)

MC68HSC705C8AP pin assignments are identical to those of the MC68HC705C8P.

C.10.2 PLCC (MC68HSC705C8AFN)

MC68HSC705C8AFN pin assignments are identical to those of the MC68HC705C8FN.

C.10.3 CERDIP MC68HSC705C8AS)

MC68HSC705C8AS pin assignments are identical to those of the MC68HC705C8S.

C.10.4 QFP (MC68HSC705C8AFB)

MC68HSC705C8AFB pin assignments, shown in Figure C-10, are identical to those of the MC68HC705C8FB.

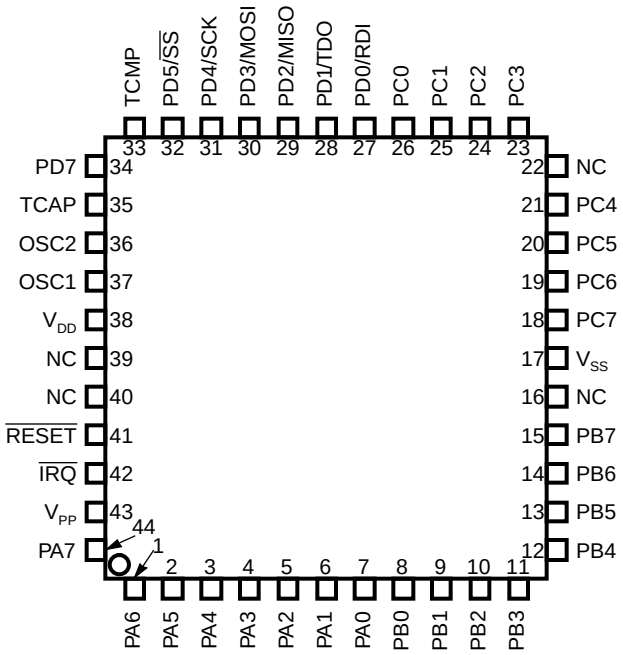


Figure C-10. MC68HSC705C8AFB Pin Assignments

C.10.5 SDIP (MC68HSC705C8AB)

MC68HSC705C8AB pin assignments, shown in Figure C-11, are identical to those of the MC68HC705C8B.

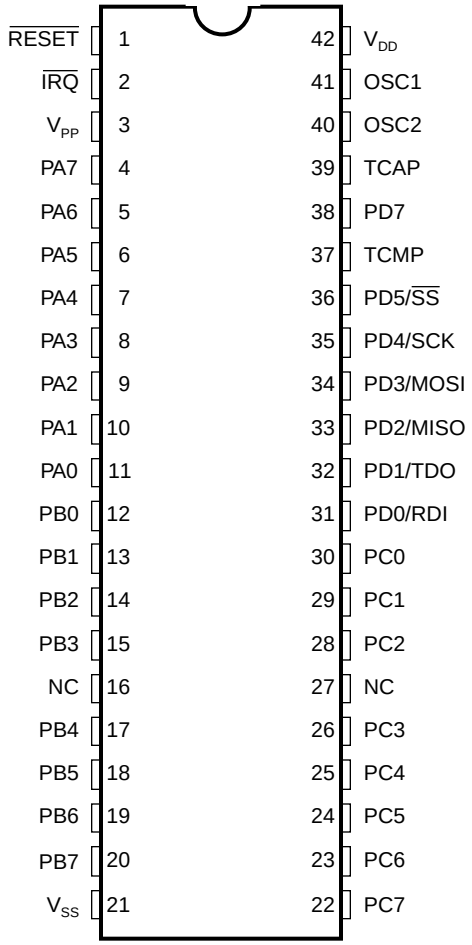


Figure C-11. MC68HSC705C8AB Pin Assignments

C.11 PACKAGE DIMENSIONS

C.11.1 DIP (MC68HSC705C8AP)

MC68HSC705C8AP dimensions are identical to those of the MC68HC705C8P.

C.11.2 PLCC (MC68HSC705C8AFN)

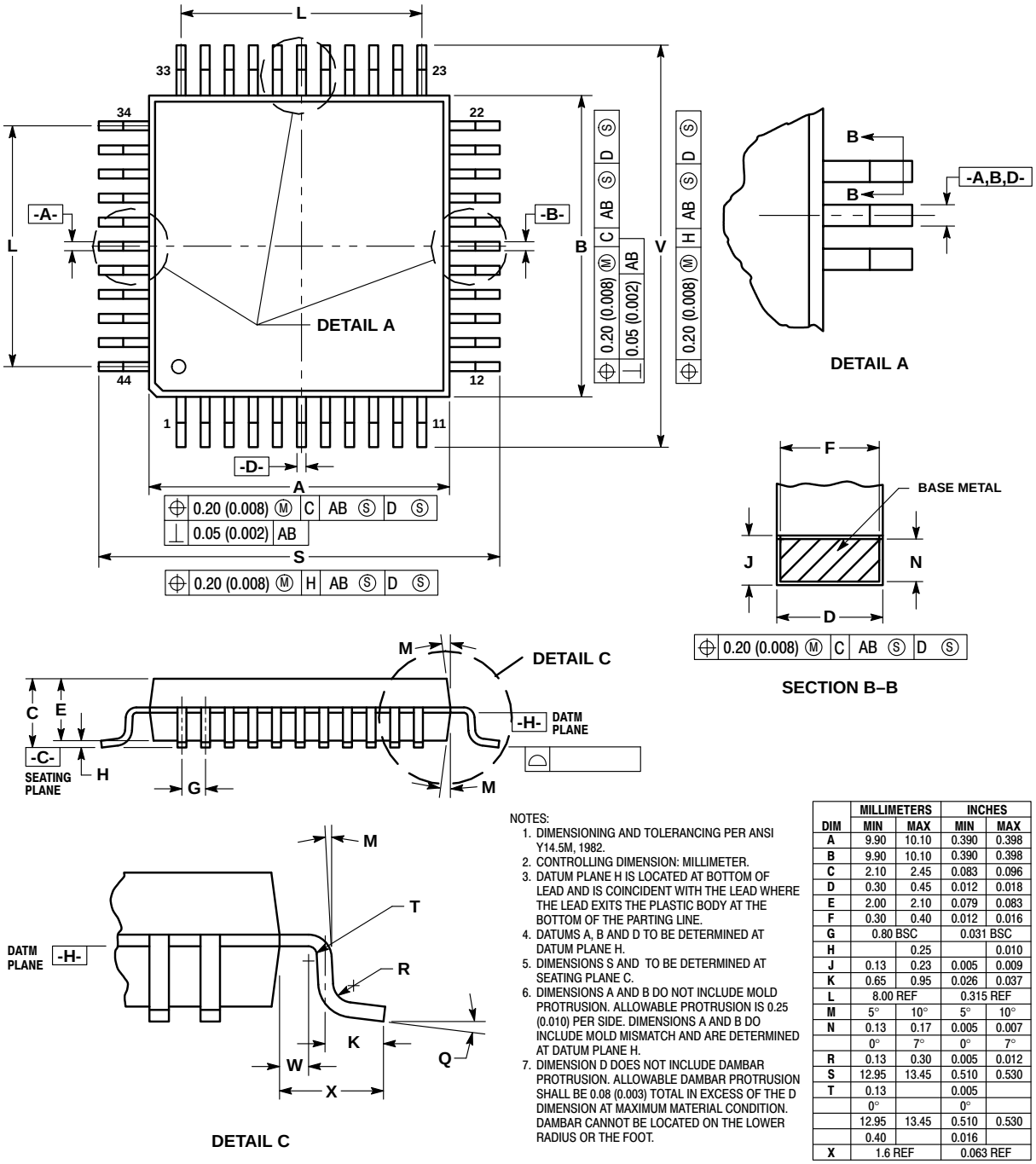
MC68HSC705C8AFN dimensions are identical to those of the MC68HC705C8FN.

C.11.3 CERDIP (MC68HSC705C8AS)

MC68HSC705C8AS dimensions are identical to those of the MC68HC705C8S.

C.11.4 QFP (MC68HSC705C8AFB)

MC68HSC705C8AFB dimensions, shown in Figure C-12, are identical to those of the MC68HC705C8FB.



NOTES:

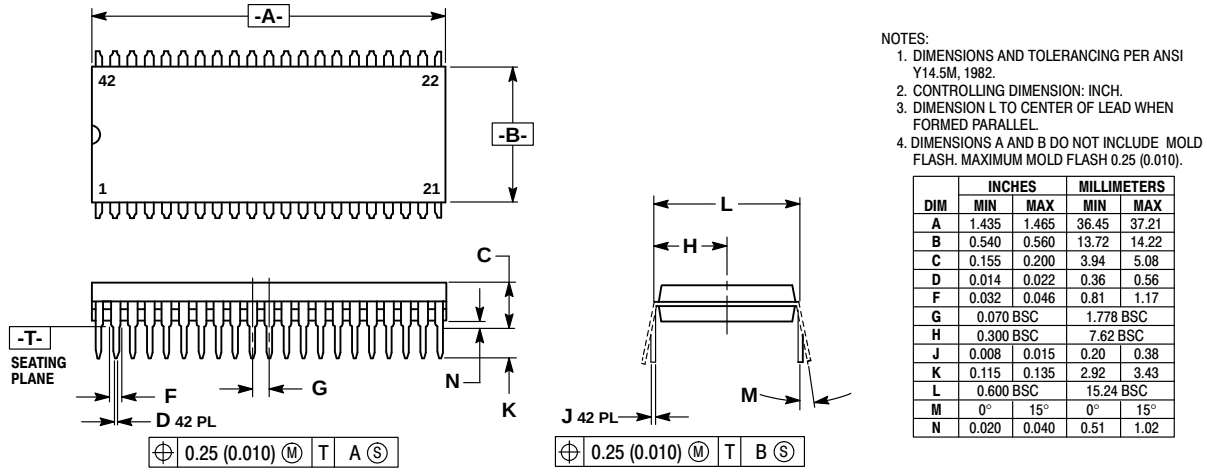
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS S AND TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.30	0.45	0.012	0.018
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
H		0.25		0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	8.00 REF		0.315 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13		0.005	
	0°		0°	
	12.95	13.45	0.510	0.530
	0.40		0.016	
X	1.6 REF		0.063 REF	

Figure C-12. MC68HSC705C8AFB Package Dimensions

C.11.5 SDIP (MC68HSC705C8AB)

MC68HSC705C8AB dimensions, shown in Figure C-13, are identical to those of the MC68HC705C8AB.



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.032	0.046	0.81	1.17
G	0.070 BSC		1.778 BSC	
H	0.300 BSC		7.62 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

Figure C-13. MC68HSC705C8AB Package Dimensions

Literature Distribution Centers:
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No.2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

MC68HC705C8AD/D